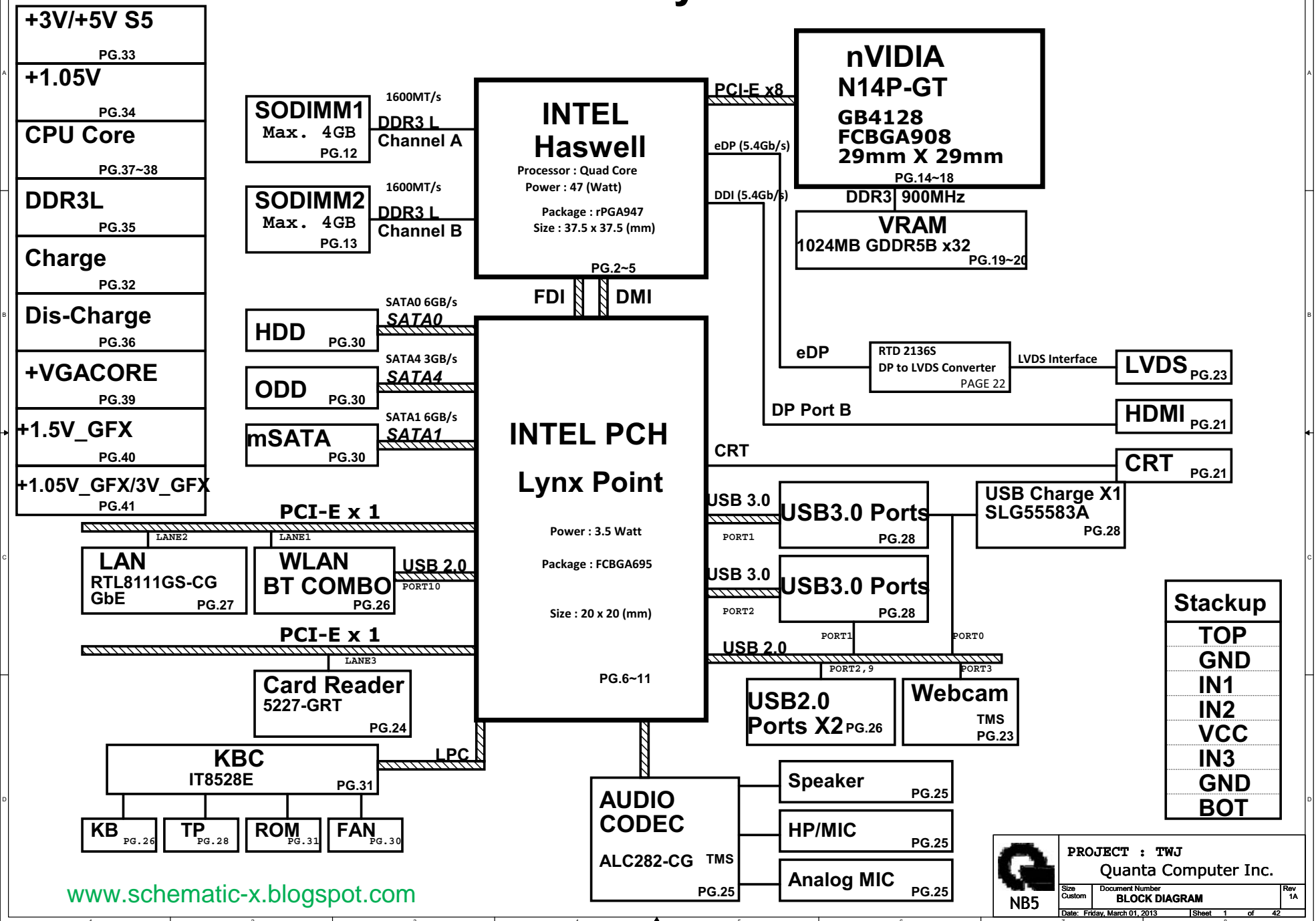


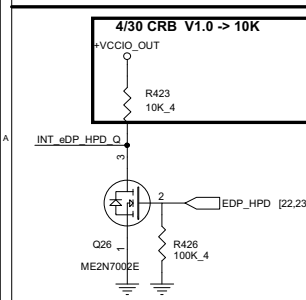
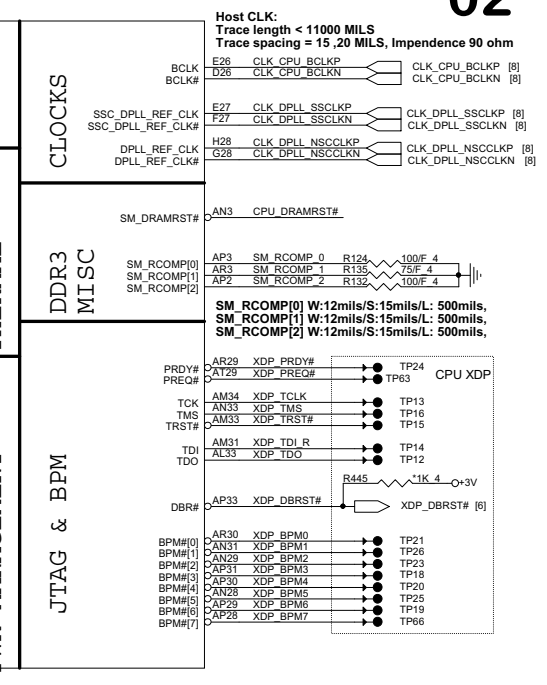
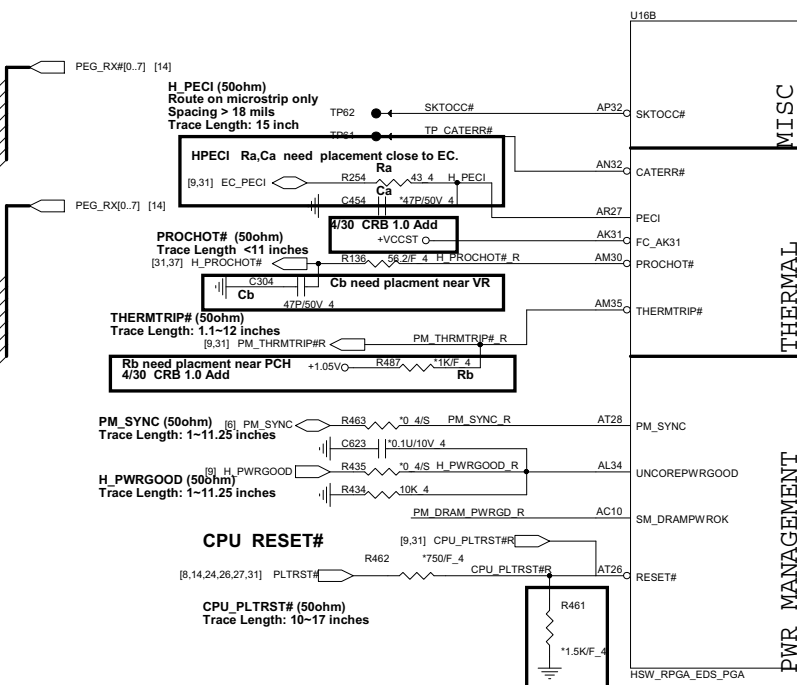
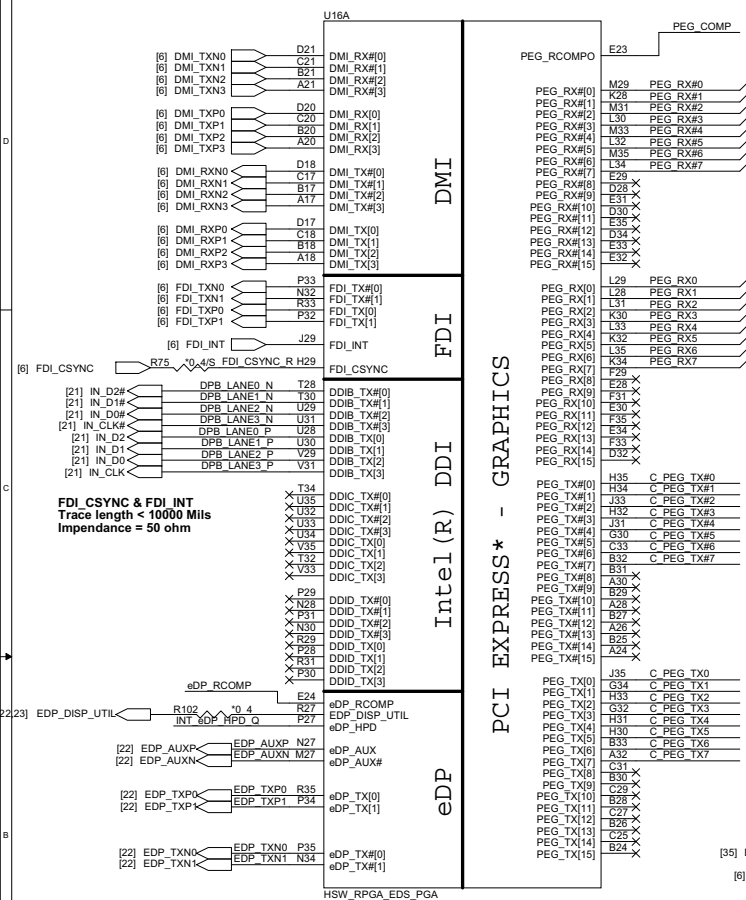
TWJ Shark Bay DIAGRAM

01

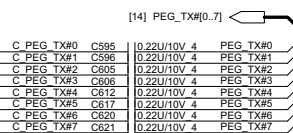
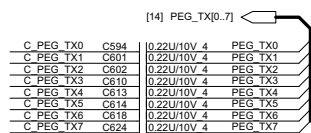


Haswell Processor (DMI, PEG, FDI)

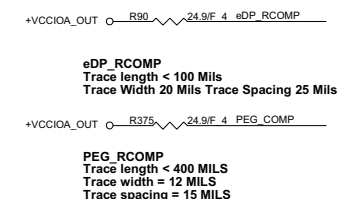
Haswell Processor (CLK, MISC, JTAG)



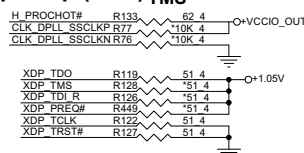
PEG x8 disable (UMA only remove)



DP & PEG Compensation TMS



Processor pull-up (CPU) TMS



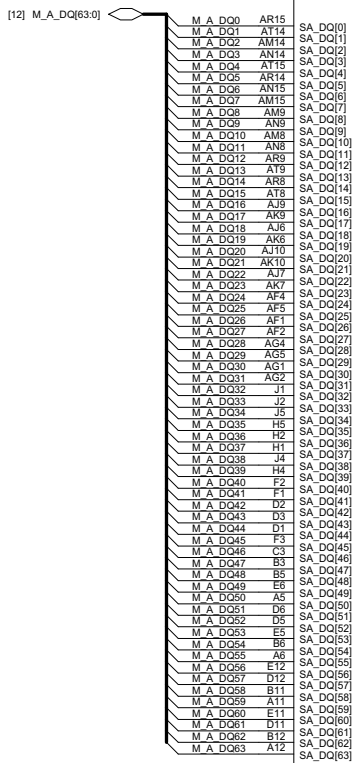
PROJECT : TWJ
Quanta Computer Inc.

Size Custom
Document Number HAS 1/4 (PCIE&DMI&FDI)
Rev 1A

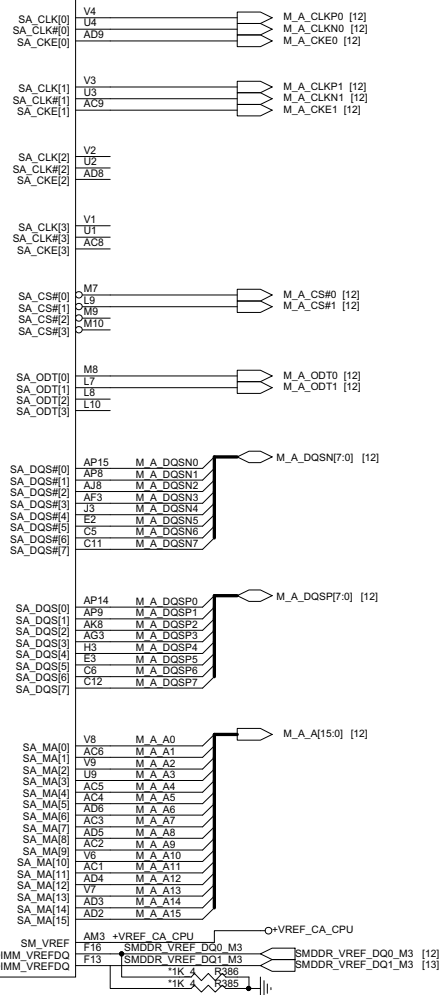
Date: Friday, March 01, 2013
Sheet 2 of 42

Haswell Processor (DDR3)

U16C



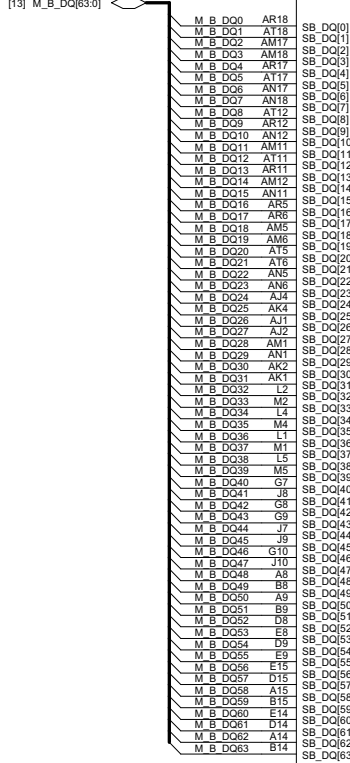
DDR SYSTEM MEMORY A



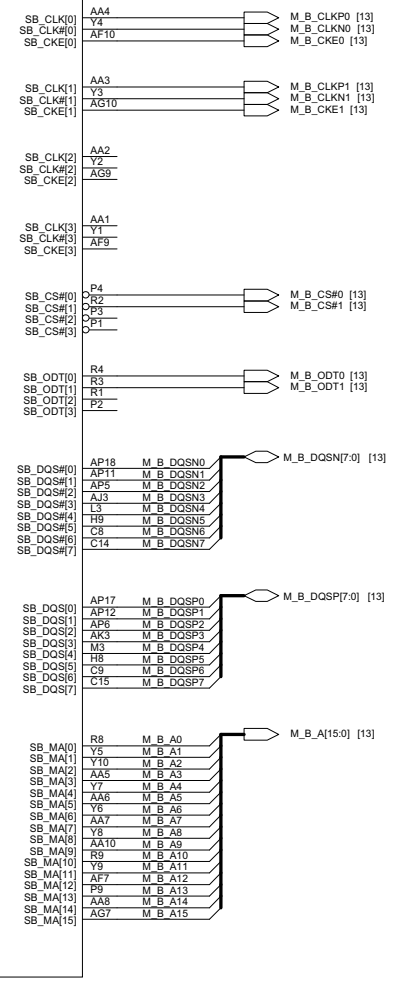
R5VD_V10 must be grounded

CPU SM_VREF

U16D



DDR SYSTEM MEMORY B



R5VD_R10 must be grounded



PROJECT : TWJ
Quanta Computer Inc.

Size Custom Document Number HAS 2/4 (DDR3 I/F) Rev 1A
Date: Friday, March 01, 2013 Sheet 3 of 42

Haswell Processor (POWER)

+VCCIN 95A

U16F

POWER

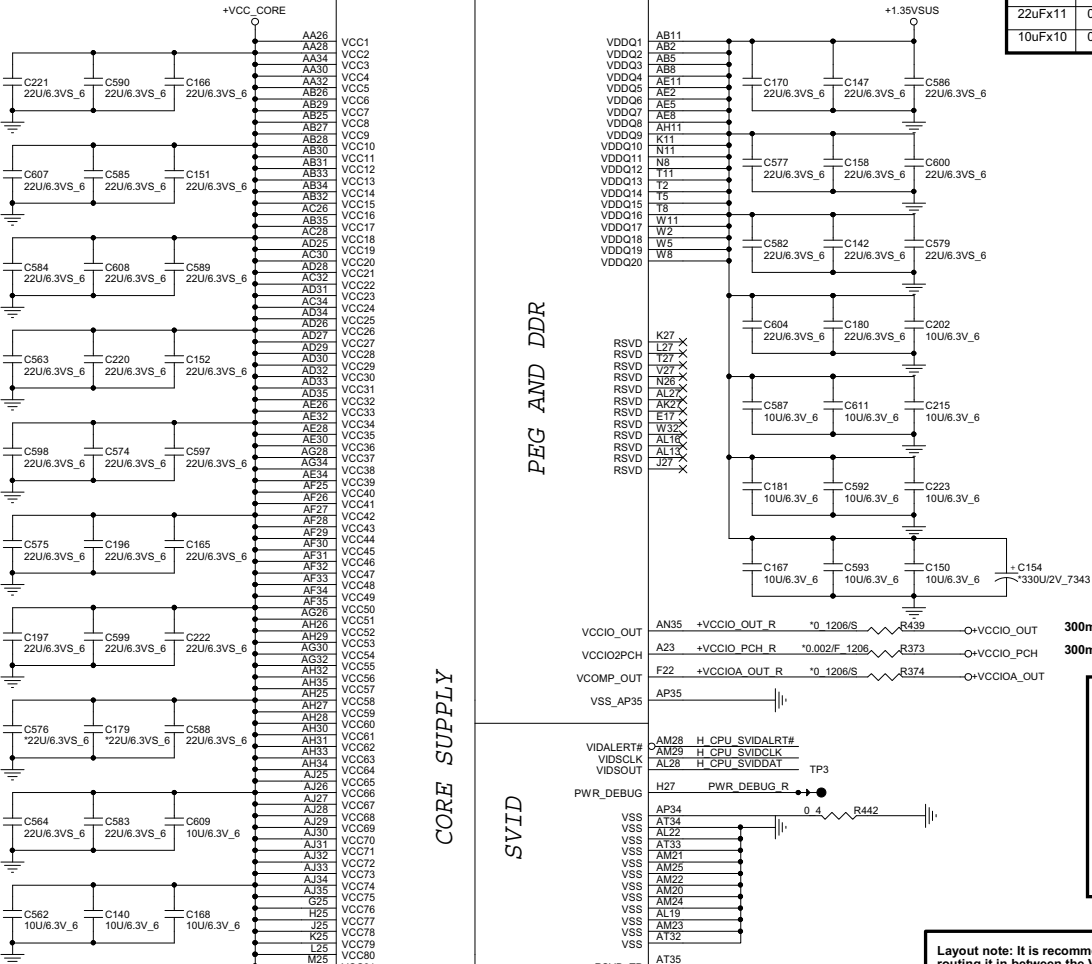
+1.35VSUS 4.2A

+1.35VSUS

VDDQ Output Decoupling Recommendations

330uFx2	7343	BOT socket side
22uFx11	0805	5 on TOP, 6 on BOT inside socket cavity
10uFx10	0805	5 on TOP, 5 on BOT inside socket cavity

+	VCCIOA_OUT [2]
+	VCCIO_PCH [10]
+	+1.5V [6,7,8,10,25,26,29,30,35]
+	+1.05V [2,7,9,10,29,34,41]
+	+VCC_CORE [37,38]
+	+VCCST [2]
+	+1.35VSUS [2,12,13,35,40]



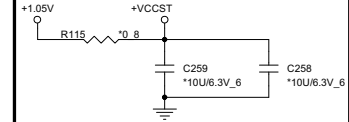
VCC Output Decoupling Recommendations		
470uFx4	7343	TOP socket side
22uFx8	0805	4 on TOP, 4 on BOT near socket edge
22uFx11	0805	TOP, inside socket cavity
10uFx11	0805	BOT, inside socket cavity

HSW_RPGA_EDS_PGA

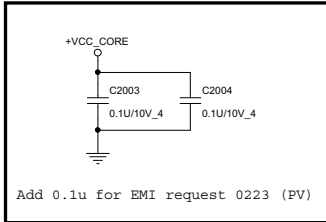
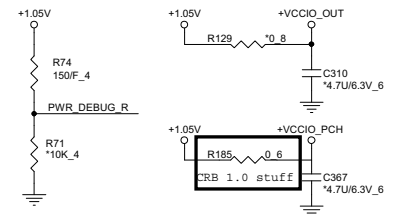
HW Thrm Protect

For 65 degree, 1.8v limit, (SW)

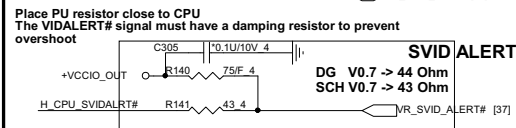
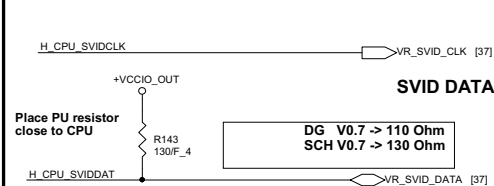
For 75 degree, 1.2v limit, (HW)



Power Test Propose



Layout note: It is recommended to shield VIDSOUT signal by routing it in between the VIDSCLK and VIDALERT# signals.



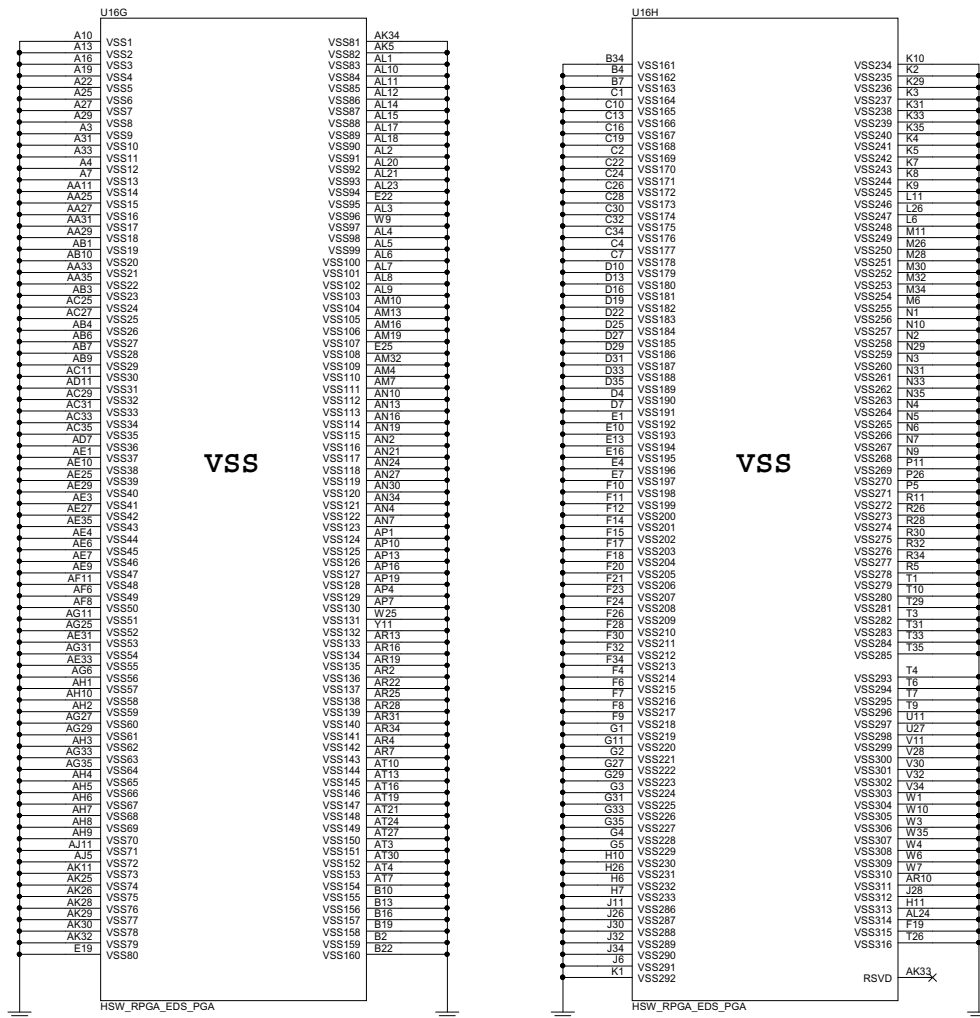
CPU VDDQ



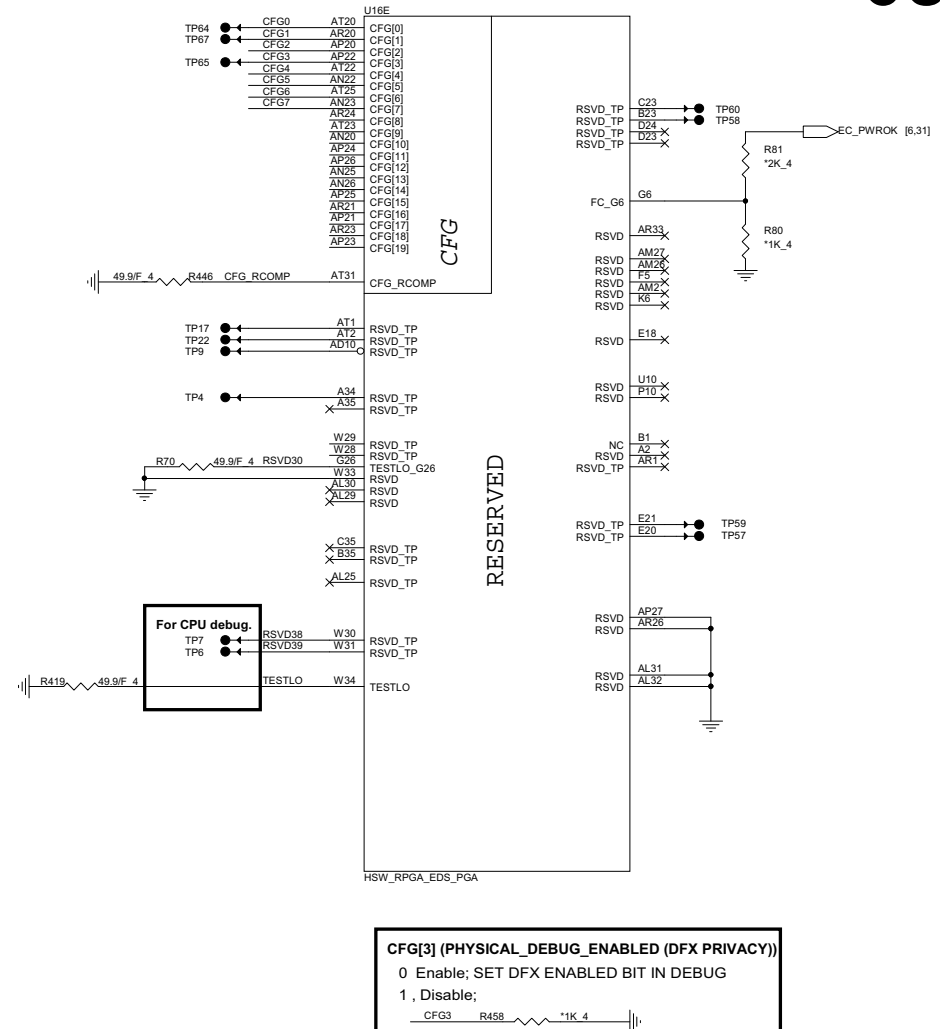
PROJECT : TWJ
Quanta Computer Inc.

Size Custom	Document Number HAS 3/4 (POWER)	Rev 1A
Date: Friday, March 01, 2013	Sheet 4	of 42

Haswell Processor (GND)



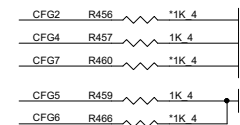
Haswell Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of "1" if not terminated on the board.

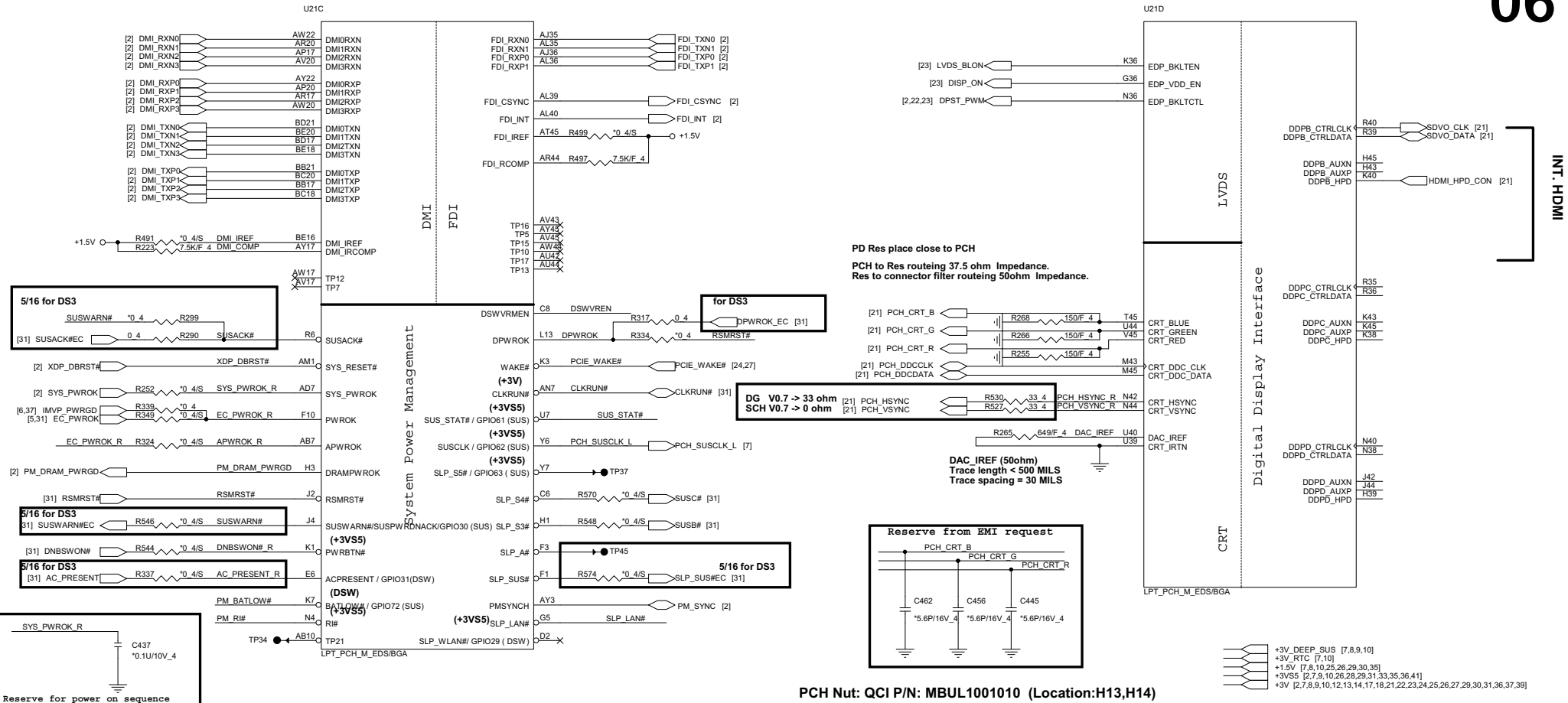
	1	0
CFG2 (PEG Static Lane Reversal)	Normal Operation	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP
CFG7 (PEG Defer Training)	PEG train immediately following xRESETB de assertion	PEG wait for BIOS training



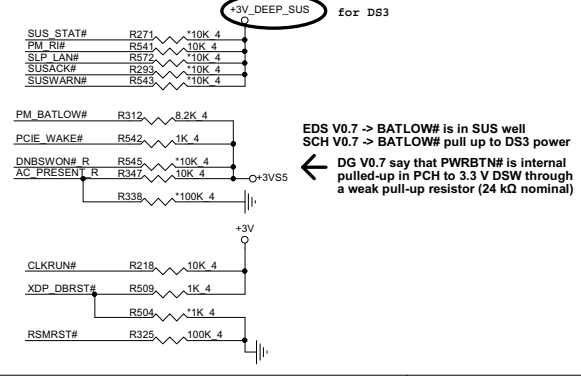
PROJECT : TWJ
Quanta Computer Inc.

Size Custom Document Number HAS 4/4 (GND) Rev 1A
Date: Friday, March 01, 2013 Sheet 5 of 42

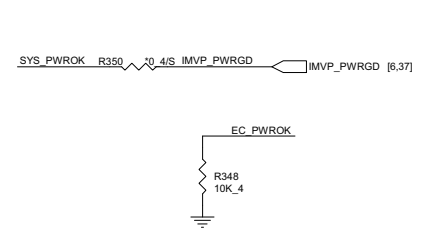
Lynx Point (DMI, FDI, PM)




PCH Pull-high/low(CLG)



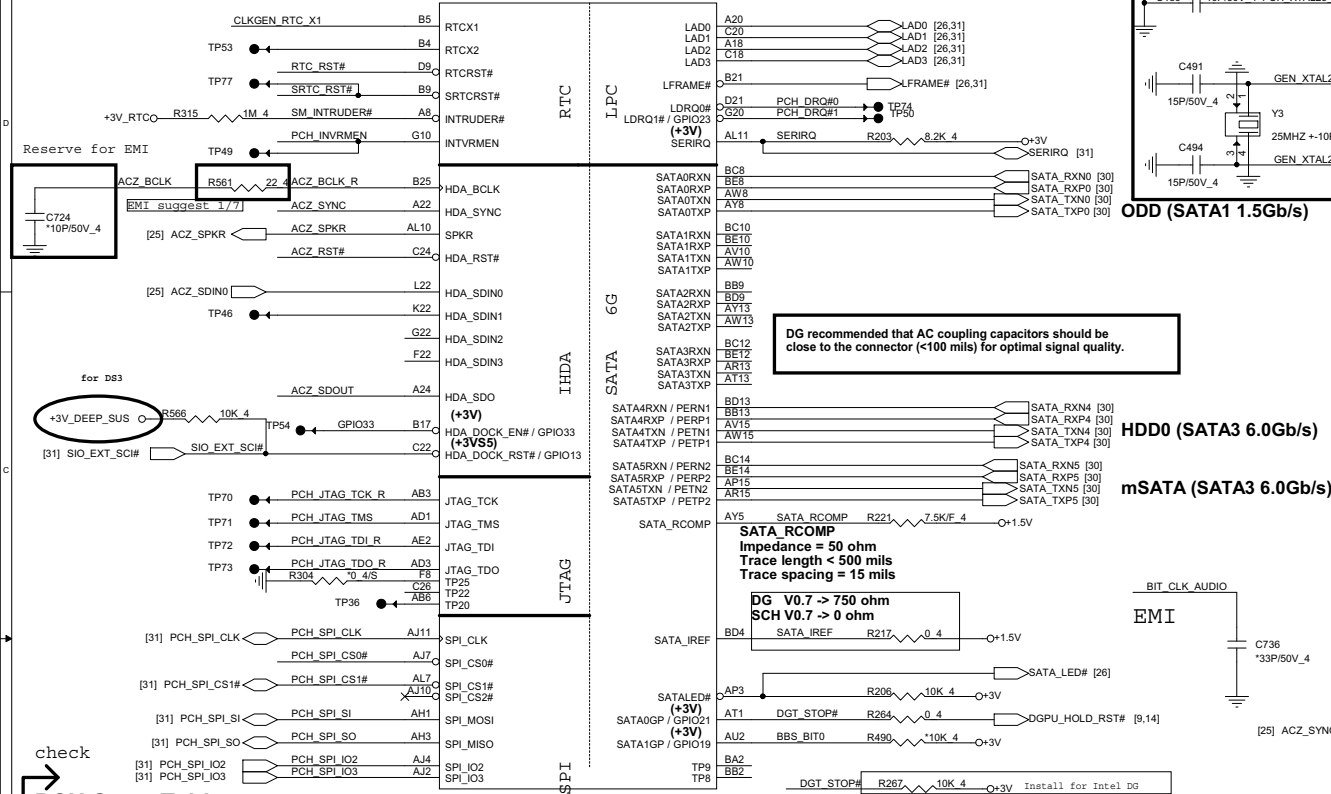
System PWR_OK(CLG)



 NB5	PROJECT : TWJ Quanta Computer Inc.			Rev
	Size Custom	Document Number PCH 1/6 (DMI/FDI/VIDEO)		1A
Date: Friday, March 01, 2013		Sheet	6	of 42

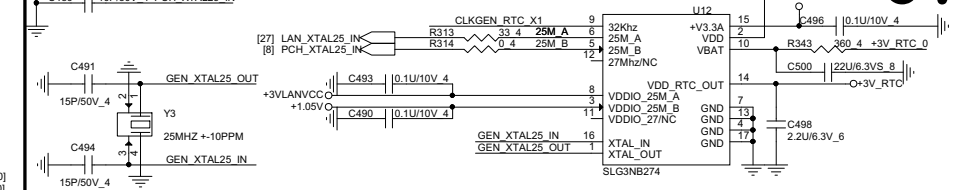
Lynx Point (HDA, JTAG, SATA)

U21A



Green CLK Circuitry RTC Clock 32.768KHz

07



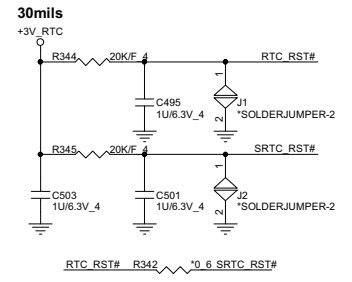
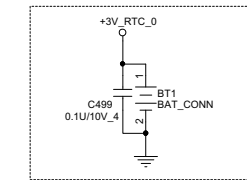
ODD (SATA1 1.5Gb/s)

HDD0 (SATA3 6.0Gb/s)

mSATA (SATA3 6.0Gb/s)

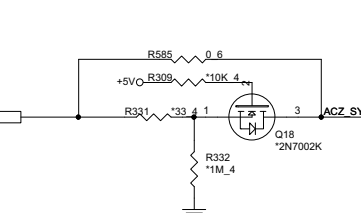
RTC Circuitry(RTC)

RTC Power trace width 20mils.
DV2...Change BT1 Pin-define

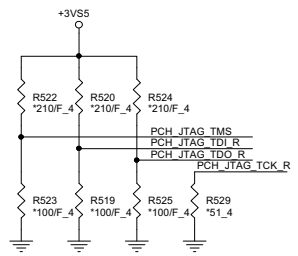


HDA Bus(CLG)

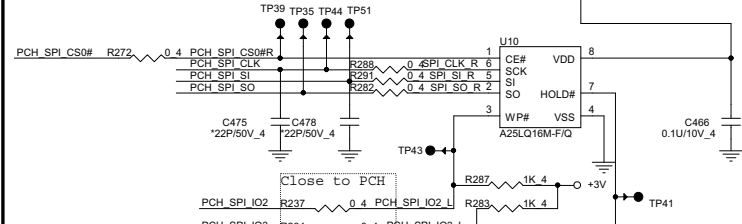
[25] BIT_CLK_AUDIO R578 33 4 ACZ_BCLK
[25] ACZ_RST#_AUDIO R584 33 4 ACZ_RST#
[25] ACZ_SDOU_AUDIO R583 33 4 ACZ_SDOU



PCH JTAG Debug(CLG)



PCH SPI ROM(CLG)



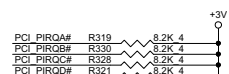
Vender	Size	P/N
AMIC	2MB	AKE38ZN0803 (AMIC A25QE16M-F/Q (QE))
Winbond	2MB	AKE38FP0N03 (Winbond W25Q16DVSSIQ)
Socket		DFHS08FS023



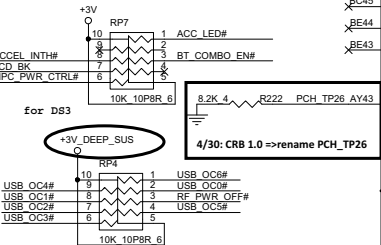
PROJECT : TWJ
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PCH 216 (SATA/HDA/SPI)	1A
Date: Friday, March 01, 2013	Sheet 7 of 42	

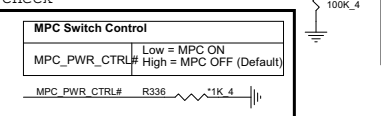
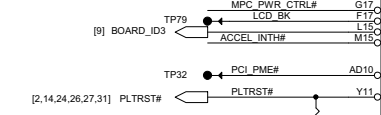
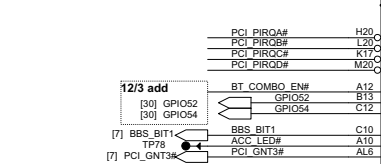
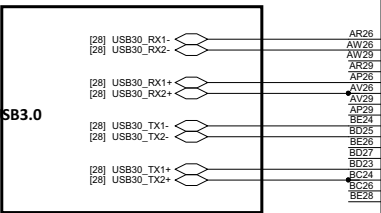
PCI/USB OC# Pull-up (CLG)



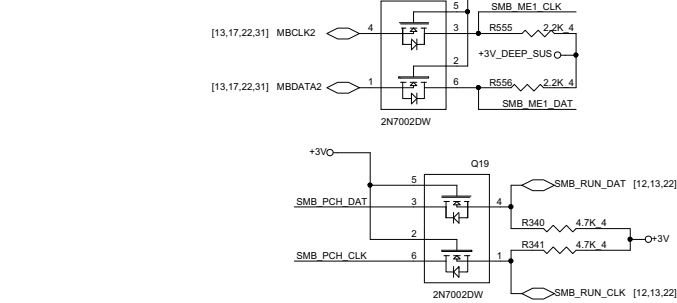
Lynx Point (PCI,USB,NVRAM)



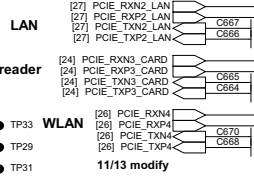
SB3.0



SMBus/Pull-up(CLG)



Lynx Point (PCI-E, SMBUS, CLK)

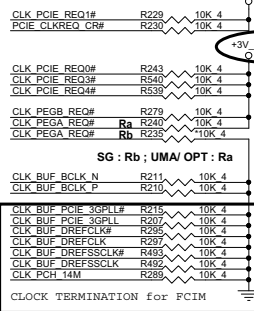


USB3.0 up
USB3.0 down
ht_USB_up +1.5V
Camera

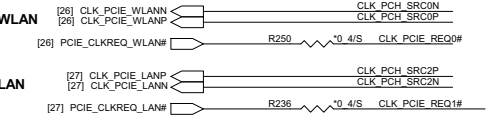
Right_USB_down
WLAN



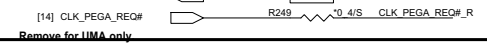
CLK REQ/Strap Pin(CLG) +3V



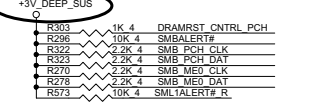
PCIE Clock



GPU

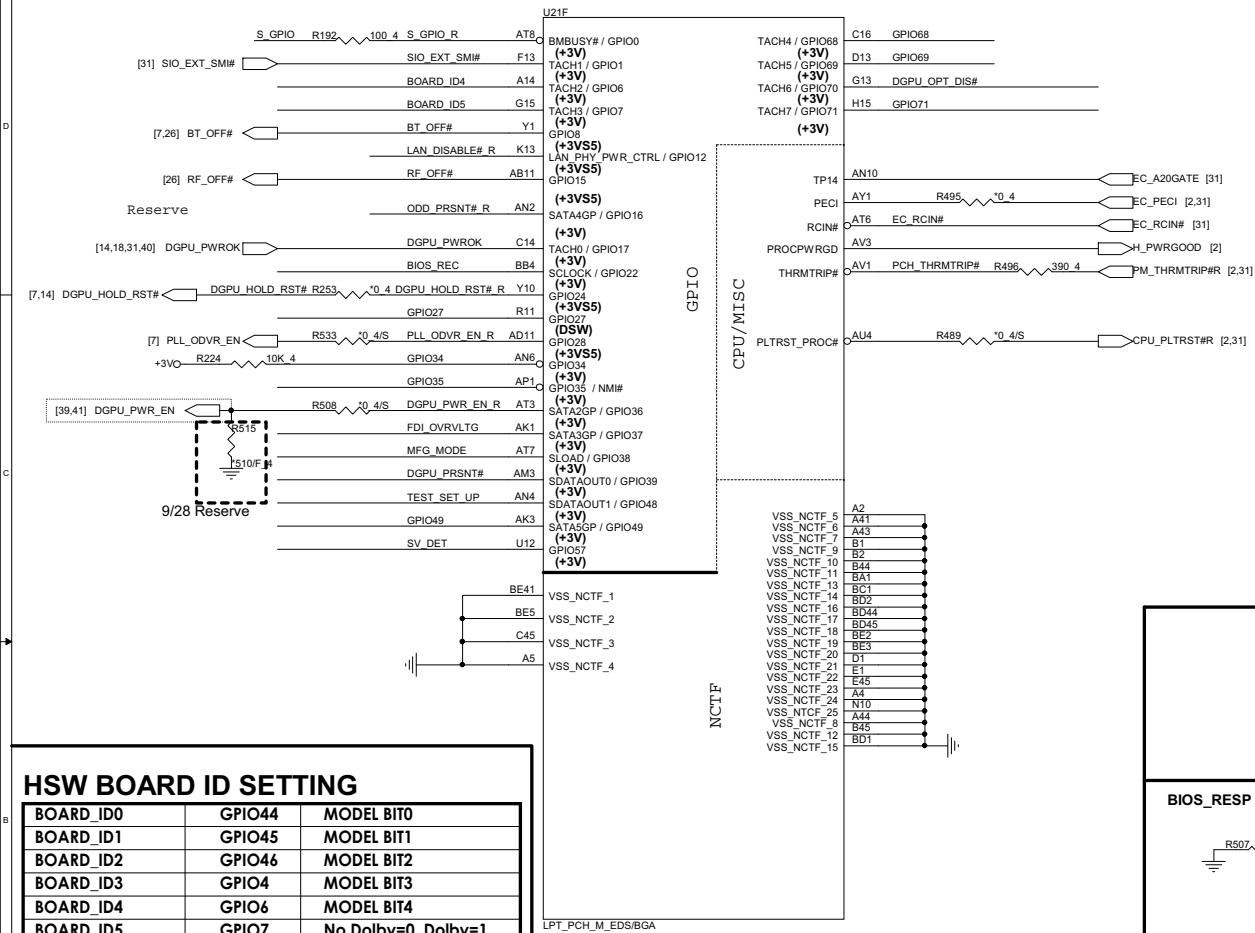


SMBus/Pull-up(CLG)



PROJECT : TWJ		
Quanta Computer Inc.		
Size Custom	Document Number PCH 3/6 (PCIE/USB/CLK)	Rev 1A

Lynx Point (GPIO,VSS_NCTF,RSVD)

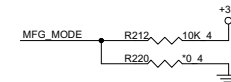


+3V_DEEP_SUS [6,7,8,10]
 +3VS5 [2,6,7,10,26,29,31,33,35,36,41]
 +3V [2,6,7,8,10,12,13,14,17,18,21,22,23,24,25,26,27,29,30,31,36,37,39]
 +5VS5 [25,29,33,34,35,36,37,38,39,40]

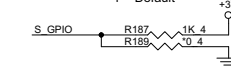
PCH MISC PU /PD



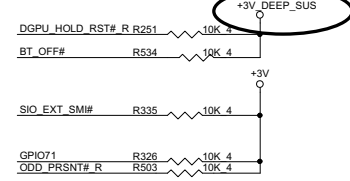
MFG-TEST



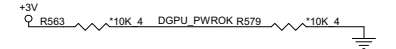
Swap GPIO



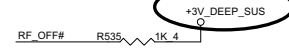
GPIO Pull-up/Pull-down(CLG) for DS3



DGPU_PWROK UMA=0

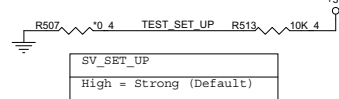


for DS3

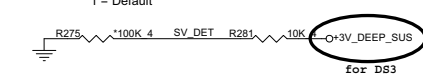


Intel ME Crypto Transport Layer
 Security (TLS) cipher suite
 Low = Disable (Default)
 High = Enable

BIOS_RESP



SV Detect

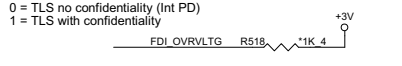


for DS3

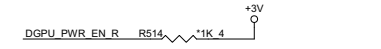
DGPU_OPT_DIS# GPIO70 Optimus=0, Dis only=1



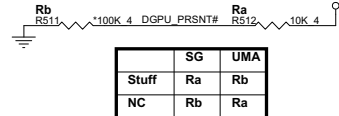
SATA3GP/GPIO37 TLS Confidentiality



GPIO36 Internal PD



GFX Present GPIO39 Optimus=1, UMA=0



SG	UMA
Stuff	Ra
NC	Rb
	Ra



PROJECT : TWJ
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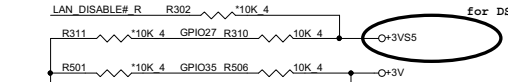
Size Custom Document Number PCH 4/6 (GPIO/MISC) Rev 1A
 Date: Friday, March 01, 2013 Sheet 9 of 42

HSW BOARD ID SETTING

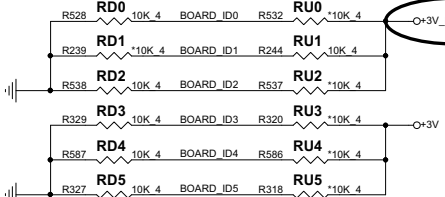
BOARD_ID0	GPIO44	MODEL BIT0
BOARD_ID1	GPIO45	MODEL BIT1
BOARD_ID2	GPIO46	MODEL BIT2
BOARD_ID3	GPIO4	MODEL BIT3
BOARD_ID4	GPIO6	MODEL BIT4
BOARD_ID5	GPIO7	No Dolby=0, Dolby=1
GPIO71	GPIO71	Reserve
GPIO35	GPIO35	Reserve
GPIO49	GPIO49	Reserve
GPIO68	GPIO68	Reserve
GPIO69	GPIO69	Reserve
DGPU_PRSTNT	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1

BOARD_ID[4:0]	Model Name
00000	QLGS
00001	TWS
00010	TWJ

GPIO68	Hi	Lo
	LVDS interface	eDP interface

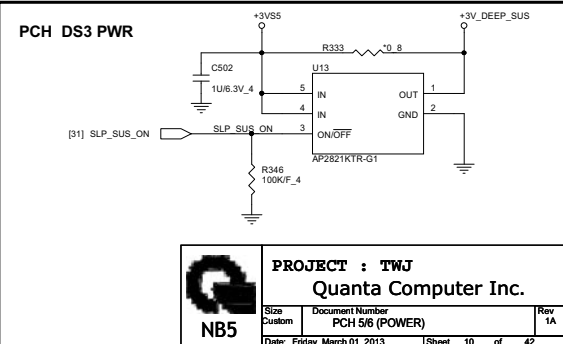
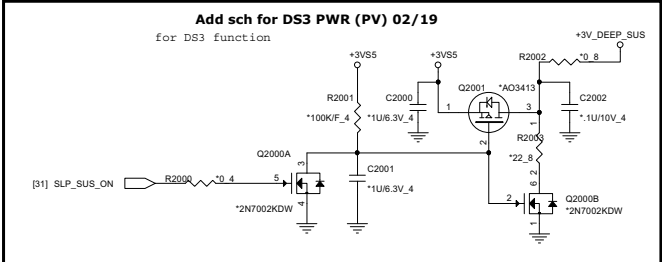
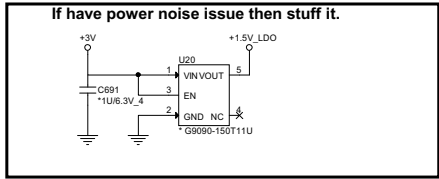


for DS3

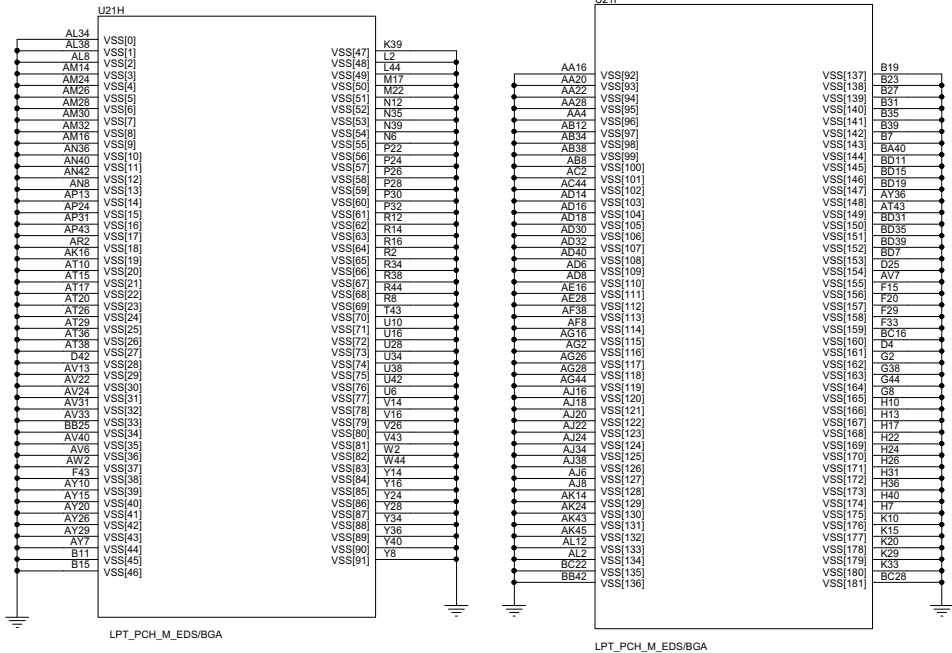


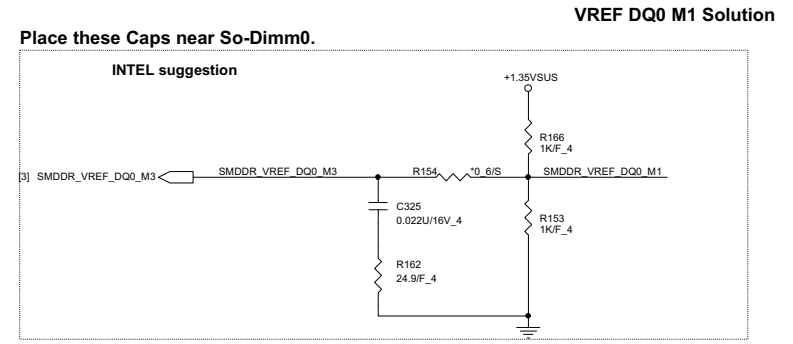
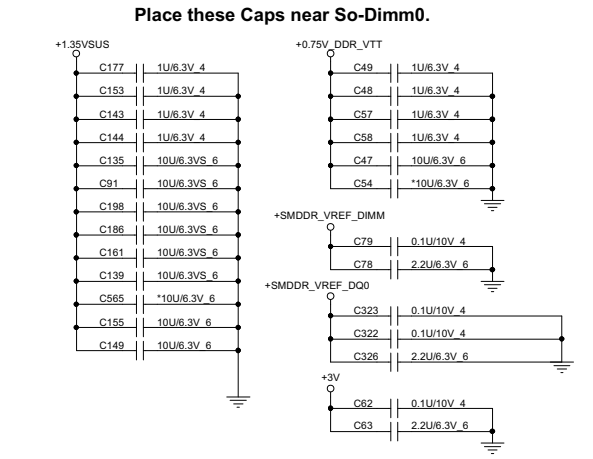
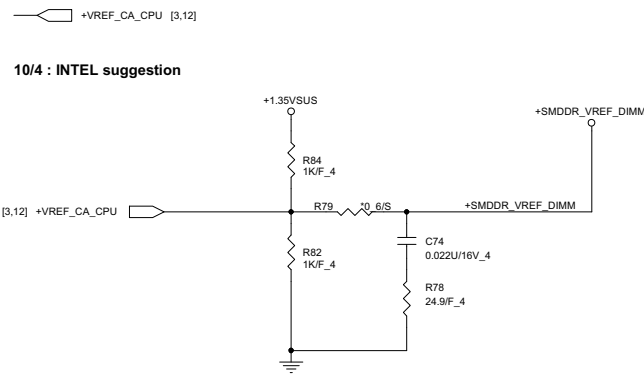
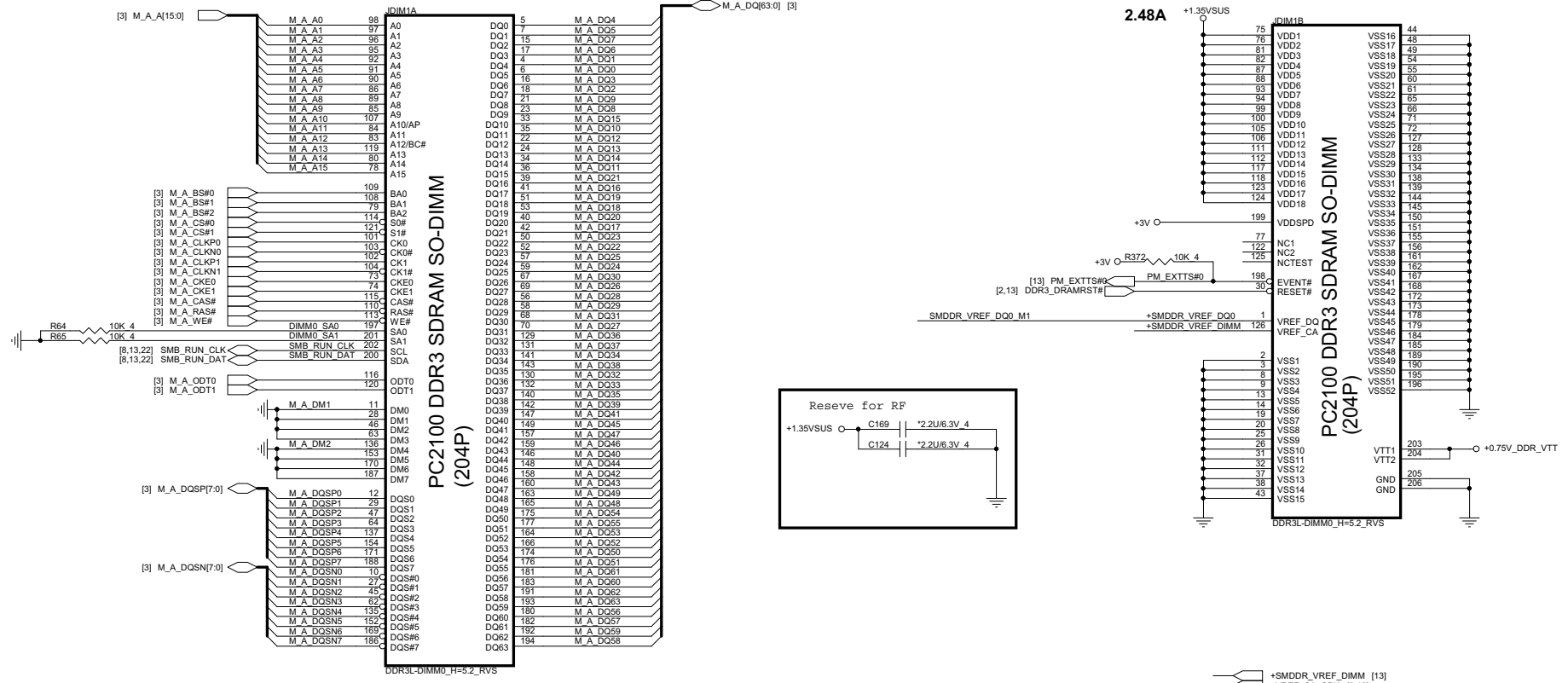
for DS3

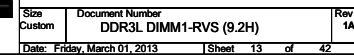
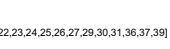
10

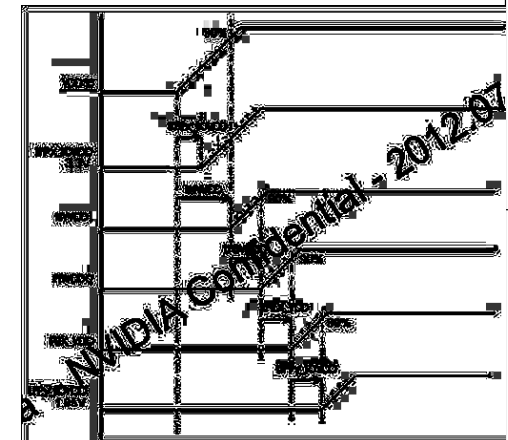
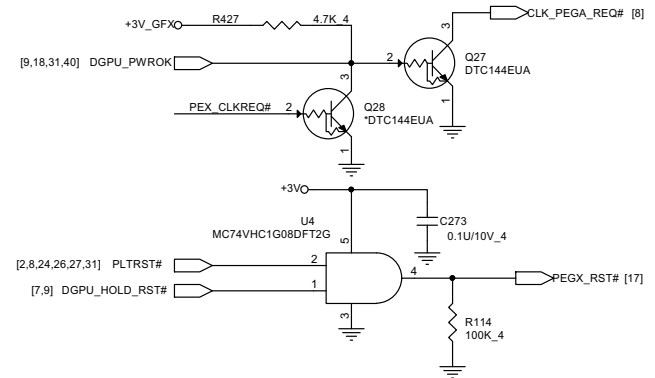
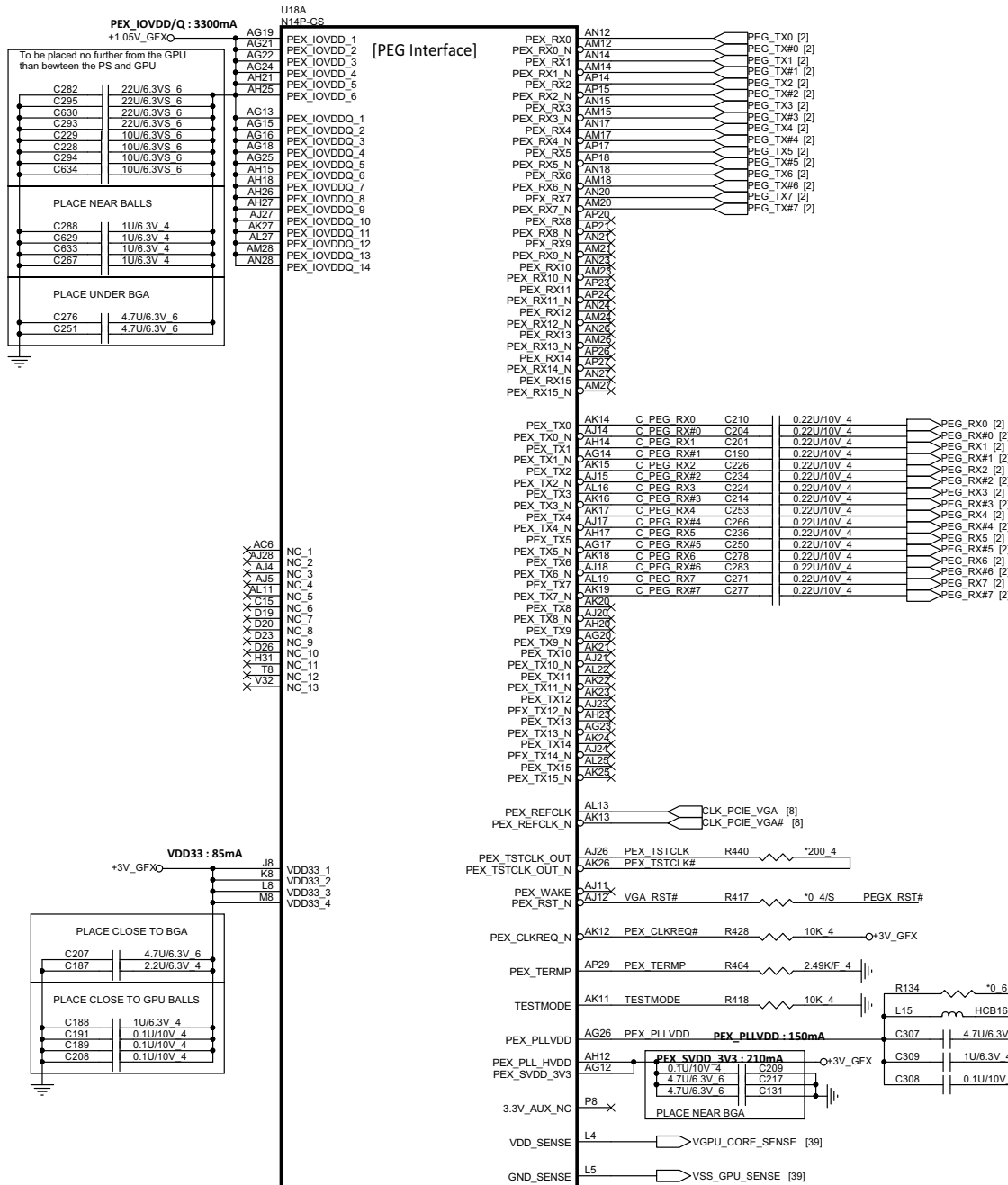


Lynx Point (GND)

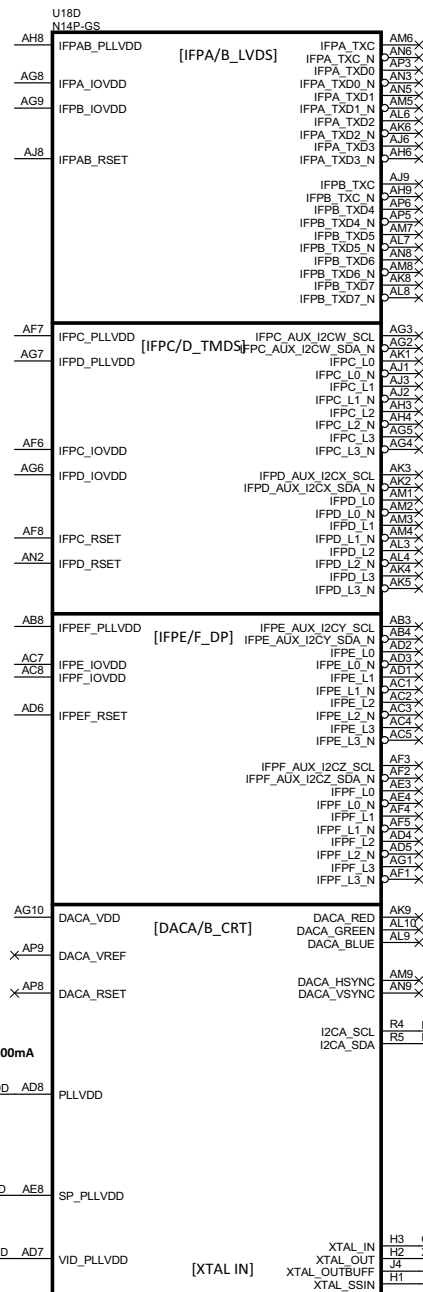




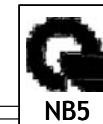
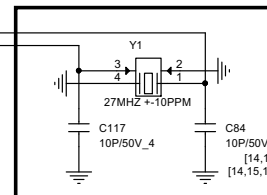








DV2...Change Y1 P/N and footprint
vendor suggest change C117,C84 to 10pf 1/11



PROJECT : TWJ
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Size A3	Document Number N14P-GT - 3/5 (Display)	Rev 1A
Date: Friday, March 01, 2013		Sheet 16 of 42

U18E
N14P-GS

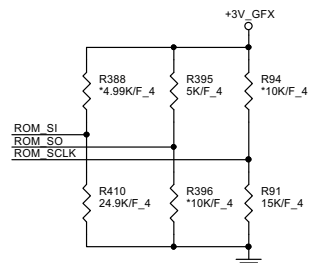
[MIOA]

[MIOB]

[MISC_GPIO/I2C/JTAG/THER]

[MISC2_ROM]

[17,40] DGPU_FB_EN



Default: GDDR5 Hynix 2G VRAM

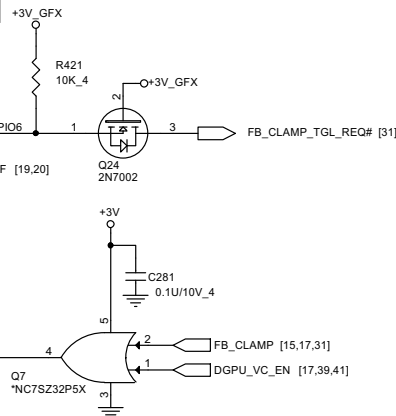
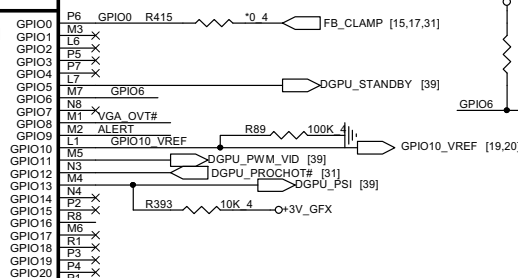
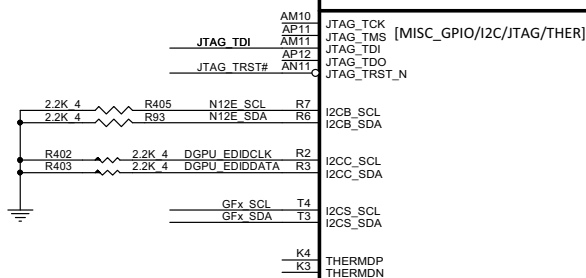
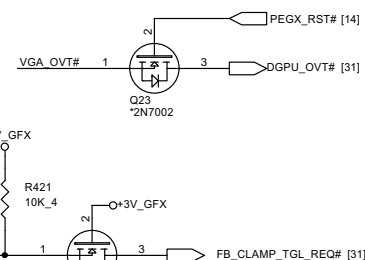
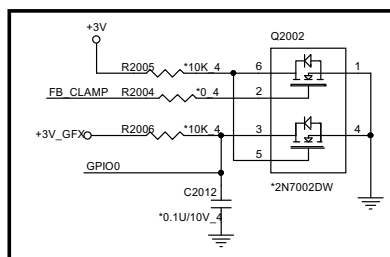
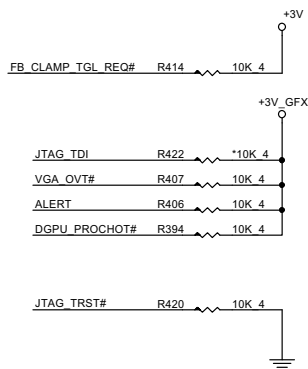
Vendor	P/N	Mfr. P/N	ROM_SI	
Hynix (1.5V)	AKG5MWUTW10	H5GQ2H24AFR-T2C	0100	24.9K PD
Hynix (1.35V)	AKG5MWUTW10	H5GQ2H24AFR-T2C	0110	34.8K PD
Samsung (1.5V)	AKG5MWDTS05	K4G20325FD-FC04	0101	30.1K PD
Samsung (1.35V)	AKG5MWDTS05	K4G20325FD-FC04	0111	45.3K PD

N14P-GT QS device ID=0x0FE4

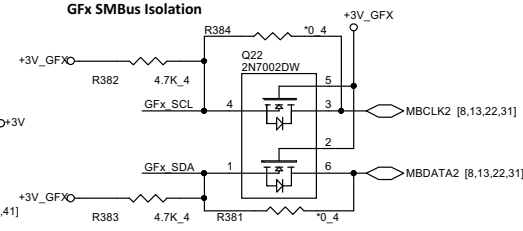
Netname	N14P-GT
ROM_SO	4.99K PU
ROM_SCLK	15K PD
STRAP0	45.3K PU
STRAP1	4.99K PD
STRAP2	24.9K PD
STRAP3	4.99K PD
STRAP4	45.3K PD

4.99K/F 4: CS24992FB26 RES CHIP 4.99K 1/16W +1% (0402)
 10K/F 4: CS31002FB26 RES CHIP 10K 1/16W +1% (0402)
 15K/F 4: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)
 20K/F 4: CS32002FB29 RES CHIP 20K 1/16W +1% (0402)
 24.9K/F 4: CS32492FB16 RES CHIP 24.9K 1/16W +1% (0402)
 30.1K/F 4: CS33012FB18 RES CHIP 30.1K 1/16W +1% (0402)
 34.8K/F 4: CS33482FB22 RES CHIP 34.8K 1/16W +1% (0402)
 45.3K/F 4: CS34532FB18 RES CHIP 45.3K 1/16W +1% (0402)

Logical Strap Bit Mapping



Gfx SMBus Isolation



GPIO ASSIGNMENTS



PROJECT : TWJ

Quanta Computer Inc.

Size Custom	Document Number N14P-GT - 4/5 (MISC)	Rev 1A
Date: Friday, March 01, 2013		Sheet 17 of 42



CHANNEL A: 1024MB GDDR5x32

19

Channel 0
<0-31>

Channel 0
<32-63>

Channel 1
<0-31>

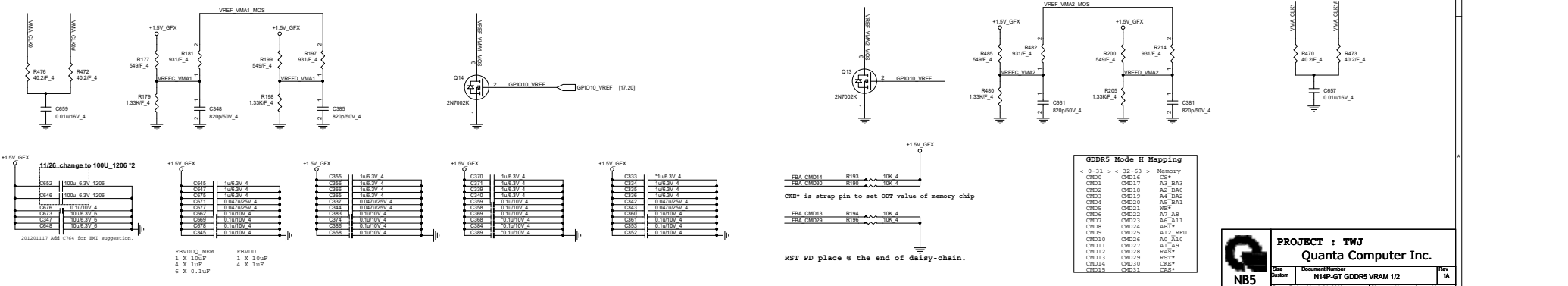
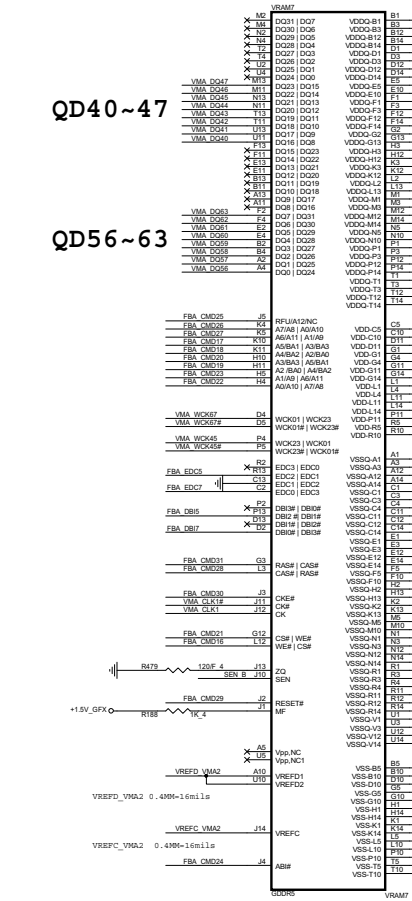
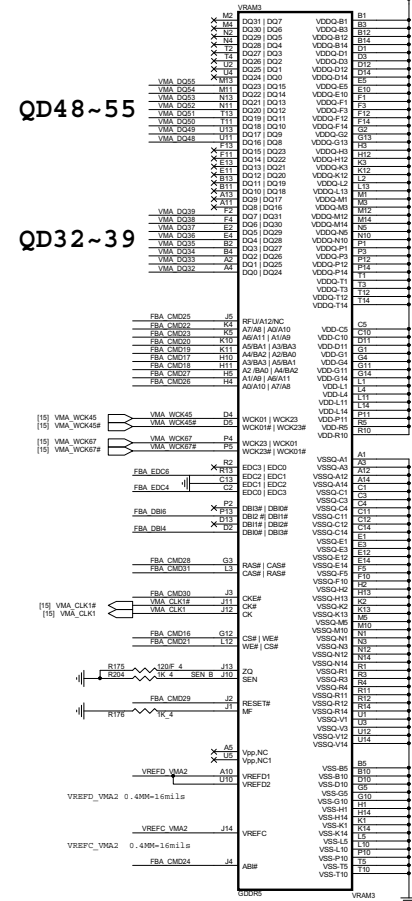
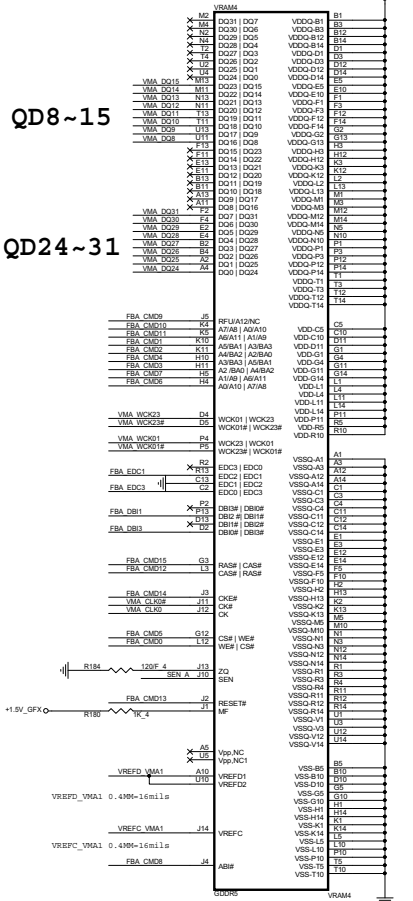
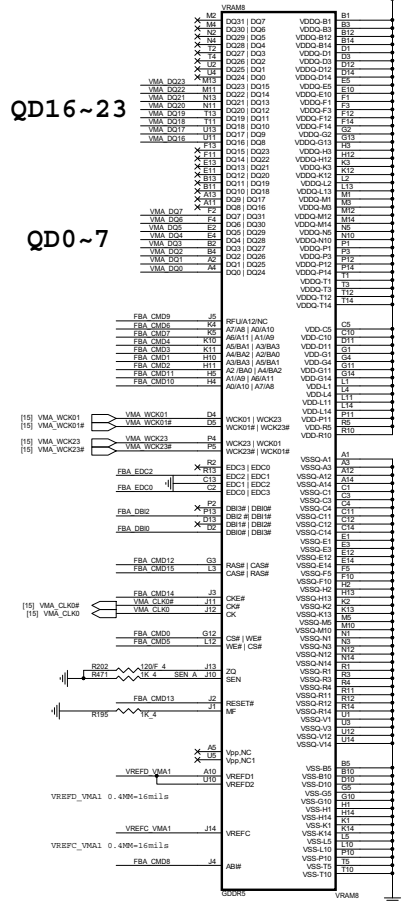
Channel 1
<32-63>

MF=0 Non-mirrored

MF=1 Mirrored

MF=0 Non-mirrored

MF=1 Mirrored



PROJECT : TWJ
Quanta Computer Inc.

Rev 1A

Doc. Friday, March 01, 2013

CHANNEL B: 1024MB GDDR5x32

20

Channel 0
<0-31>

Channel 0
<32-63>

Channel 1
<0-31>

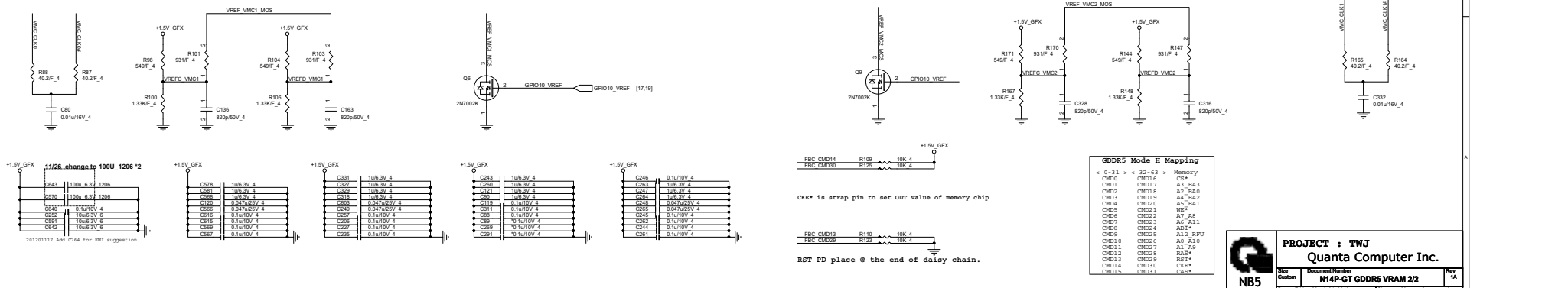
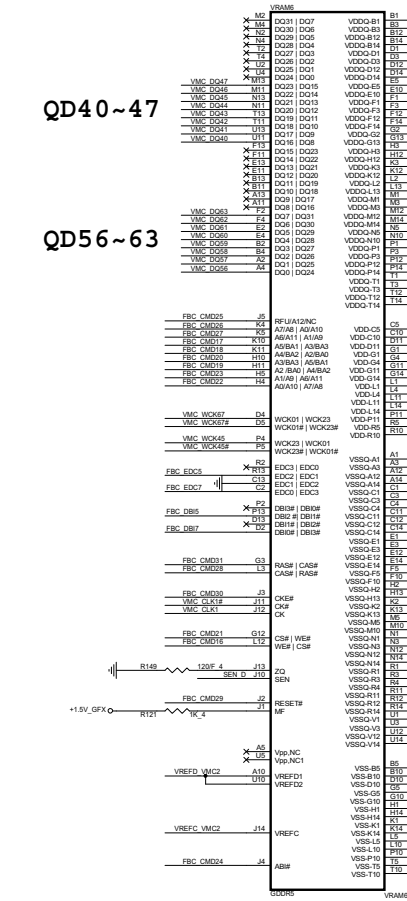
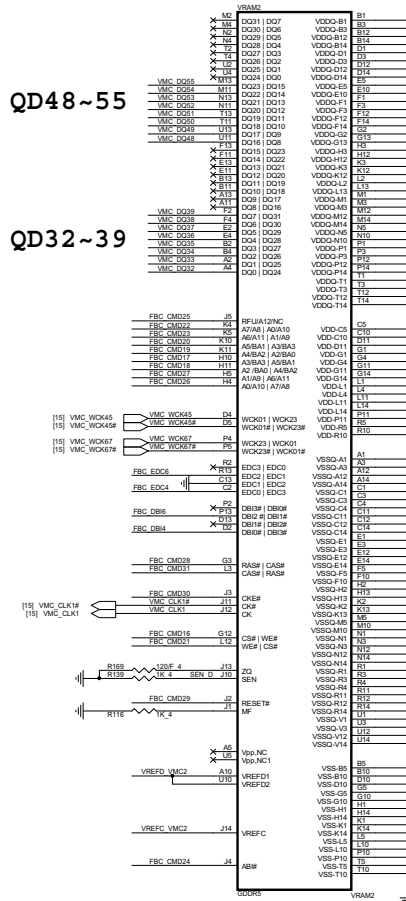
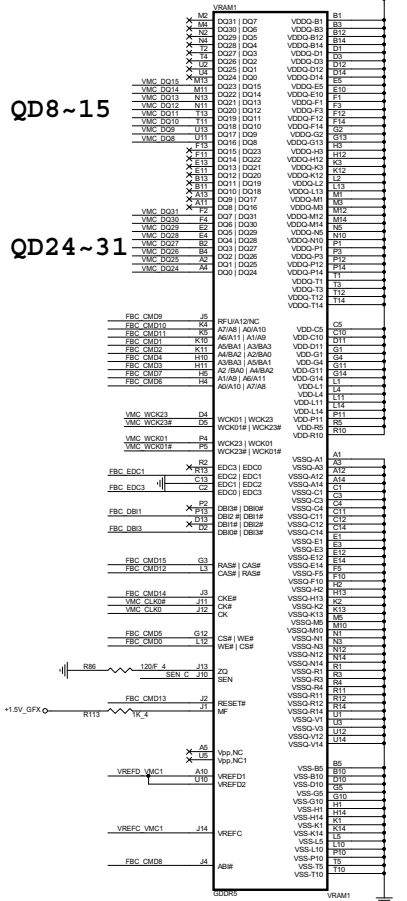
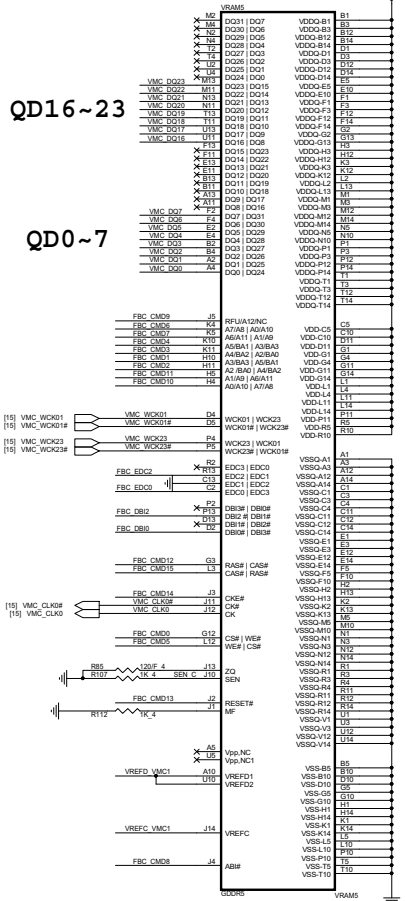
Channel 1
<32-63>

MF=0 Non-mirrored

MF=1 Mirrored

MF=0 Non-mirrored

MF=1 Mirrored

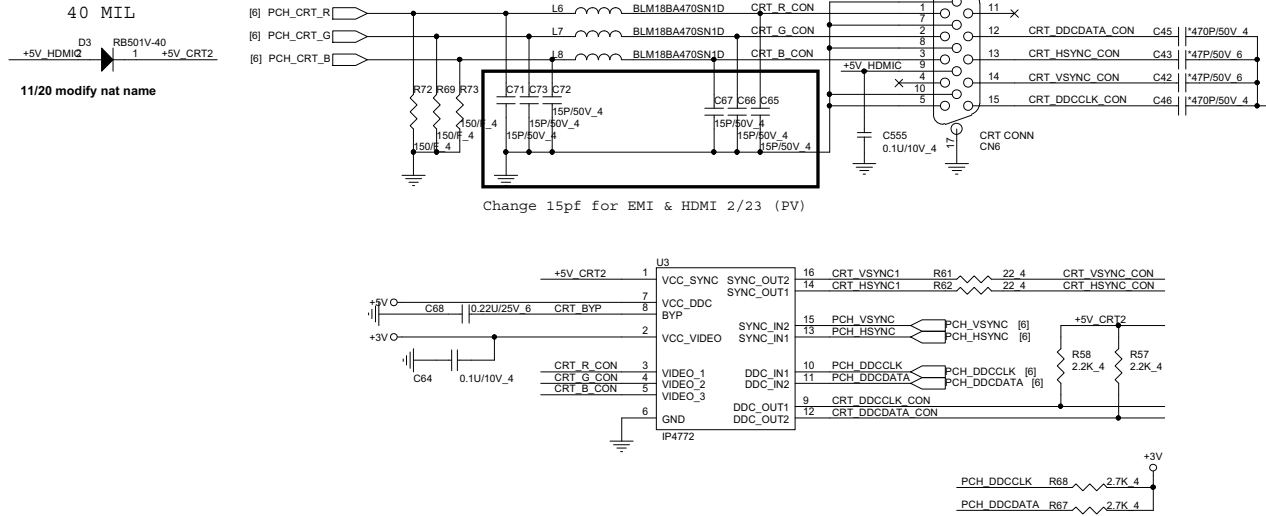


PROJECT : TWJ
Quanta Computer Inc.

Rev: 1A
Date: Friday, March 01, 2019

CRT PORT

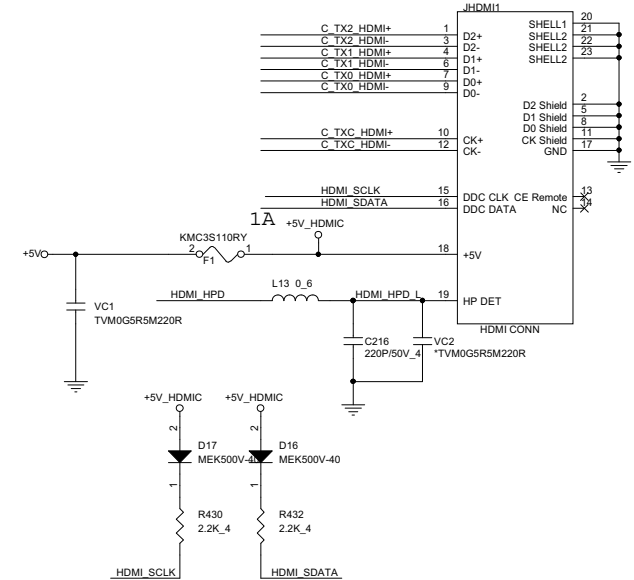
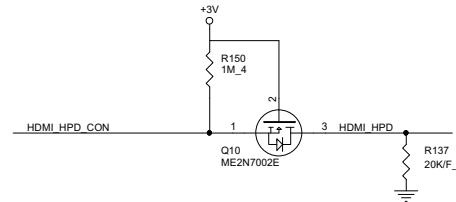
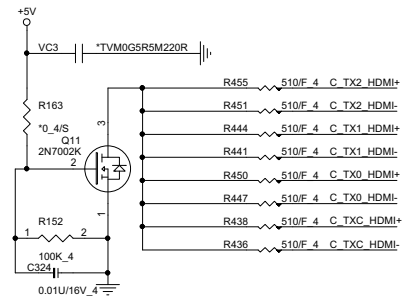
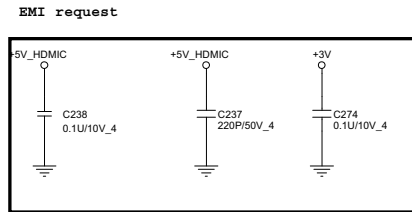
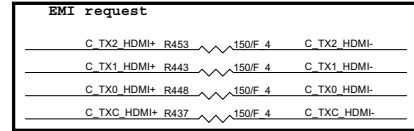
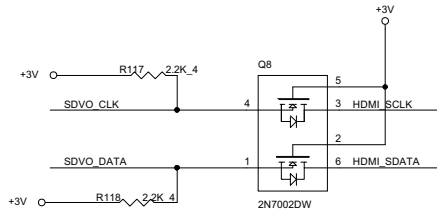
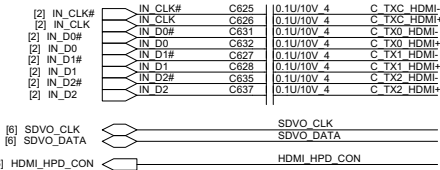
21



HDMI PORT

close to HDMI conn

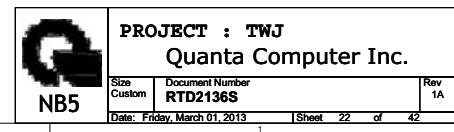
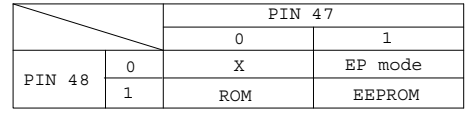
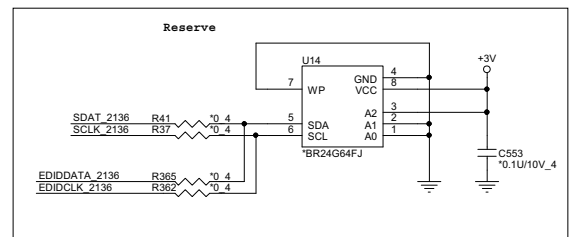
Close to HDMI Connector



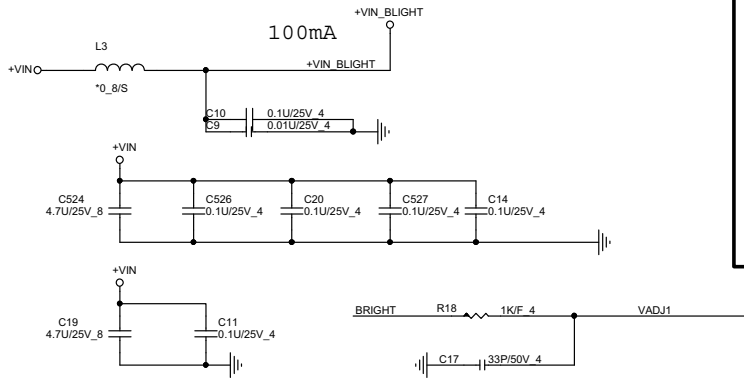
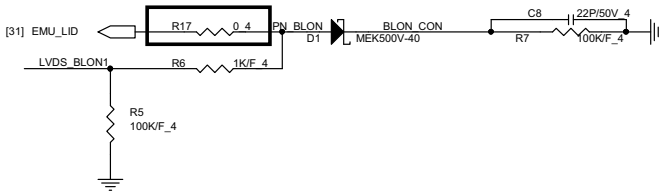
PROJECT : TWJ
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CRT_Hole	1A
Date: Friday, March 01, 2013	Sheet 21 of 42	

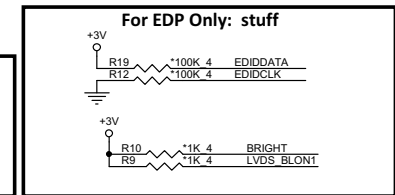
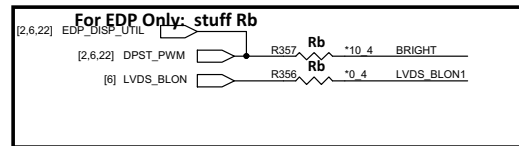
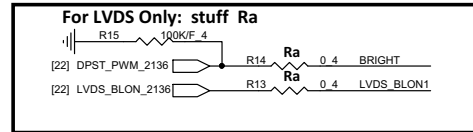
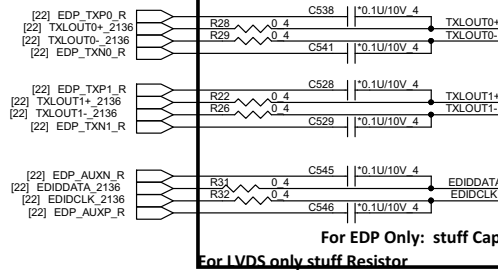
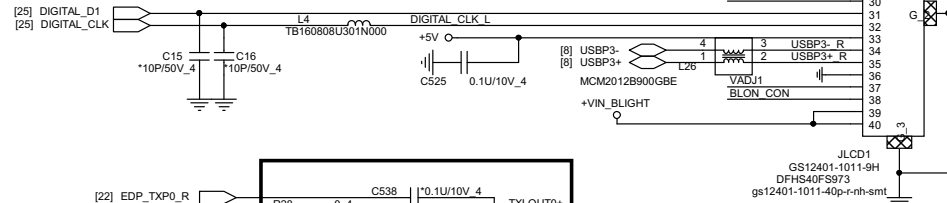
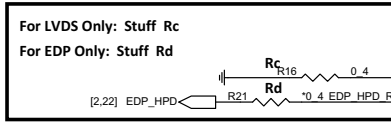
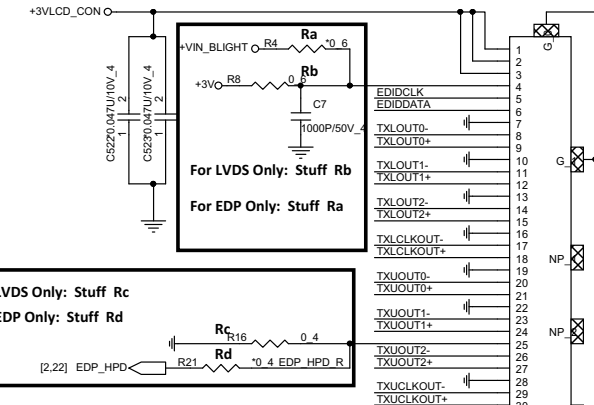
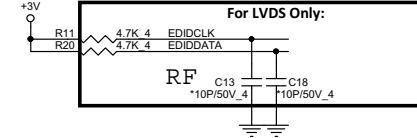
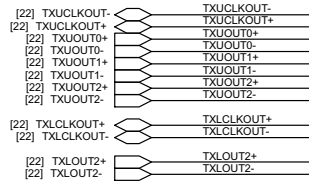
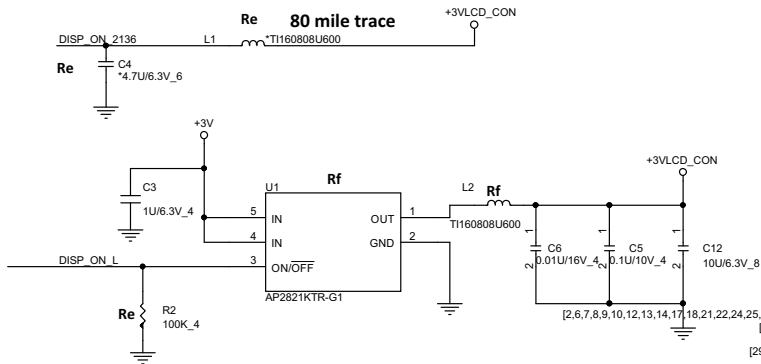
22



LID Switch

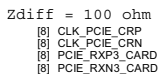


For EDP Only: stuff Rd,Rf
For LVDS Only use power switch: stuff Rc,Rf
For LVDS Only non-use power switch: stuff Re

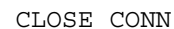


PROJECT : TWJ
Quanta Computer Inc.

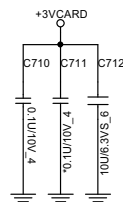
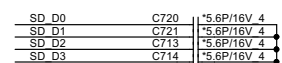
Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A
Date: Friday, March 01, 2013	Sheet 23 of 42	



SD / MMC
CARD READER



Reserve for EMI



[2,6,7,9,10,26,28,29,31,33,35,36,41] +3VS5
[2,6,7,8,9,10,12,13,14,17,18,21,22,23,25,26,27,29,30,31,36,37,39] +3V



PROJECT : TWJ
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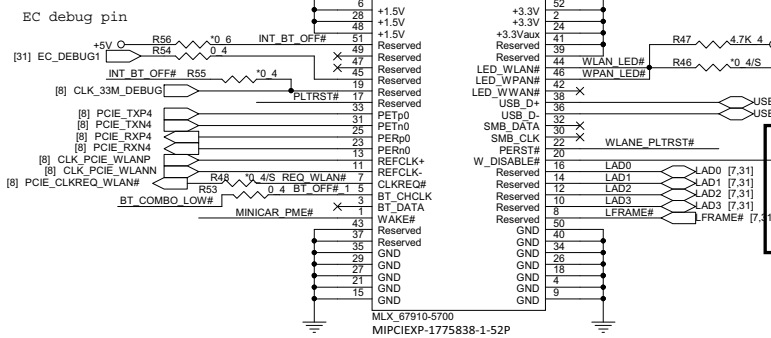
Size Custom	Document Number RTS5227 & CR SOCKET
Date: Friday, March 01, 2013	Sheet 24 of 4



PROJECT : TWJ
Quanta Computer Inc.

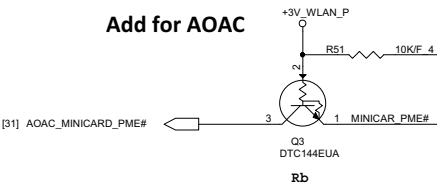
Size Custom	Document Number Azalia ALC282-CG	Rev 1A
Date: Friday, March 01, 2013	Sheet 25	of 42

**Mini Card
WLAN/BT(Optional)**

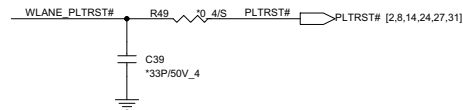


Support Wake Function(Reserve)

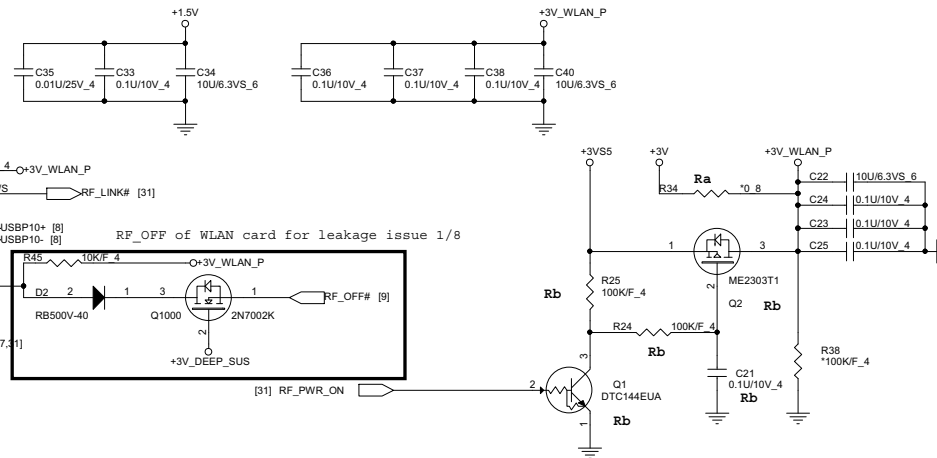
Add for AOAC



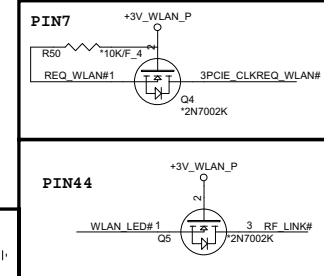
Mini Card Reset



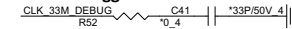
non-AOAC	LG	Ra
AOAC	CB	Rb



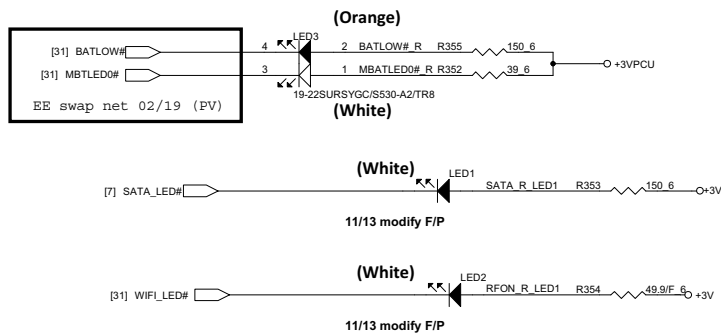
Avoid leakage issue



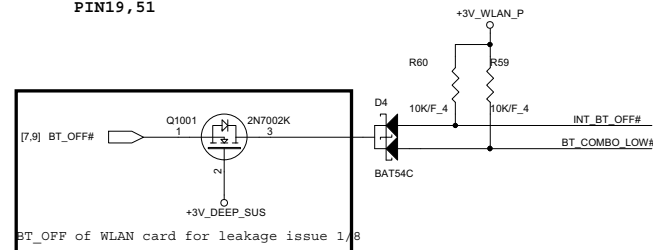
For EMI Suggestion



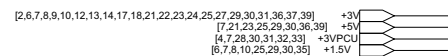
LED Status



PIN19, 51



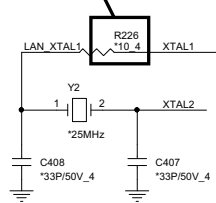
9/4 Intel COMBO card control circuit
1.add R1001,R1002,Q1001
2.add net name"INT_BT_COMBO_EN#" -> "INT_BT_OFF#"



PROJECT : TWJ
Quanta Computer Inc.

Size Custom	Document Number MINI PCIE CONN & LED	Rev 1A
Date: Friday, March 01, 2013		Sheet 26 of 42

For EMI 0 ~ 22 ohm



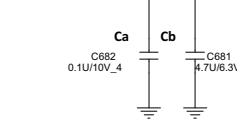
Power trace Layout 宽度 > 60mil

next ver need to add 0805 0 ohm & 0.1u cap for 10/100

>60mil

Trace < 30 mil

Width > 60 mil

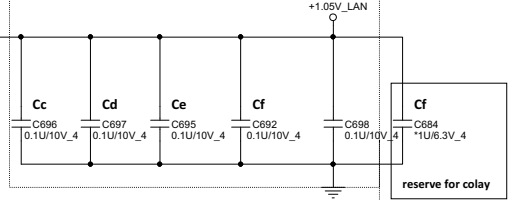


For GbE
Stuff La, Ca, Cb

For 10/100
NA: La, Ca, Cb

For GbE
* Place Cc, Cd, Ce, Cf, Cg
close to each VDD10 pin-- 3, 8, 22, 30

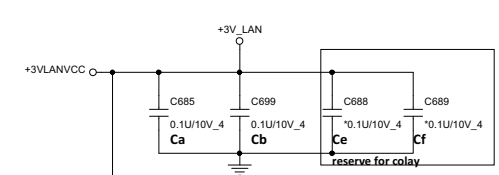
For 10/100 NA Ce, Cf
* Place Cc, Cd
close to each VDD10 pin-- 8, 30 only,



For 10/100
* Place Cf close to each VDD10 pin-- 30 (reserve)

For 10/100
* Stuff Ce and Cf only, close to each VDD33 pin-- 23, 32

For GIGA
* Stuff Ca and Cb only, close to each VDD33 pin-- 11, 32



* Place Cc and Cd close to each VDD33 pin-- 23, 32

For GIGA
Stuff Cc, Cd

For 10/100
NA: Cc, Cd

Remove For Not Using SWR mode

For GiGa

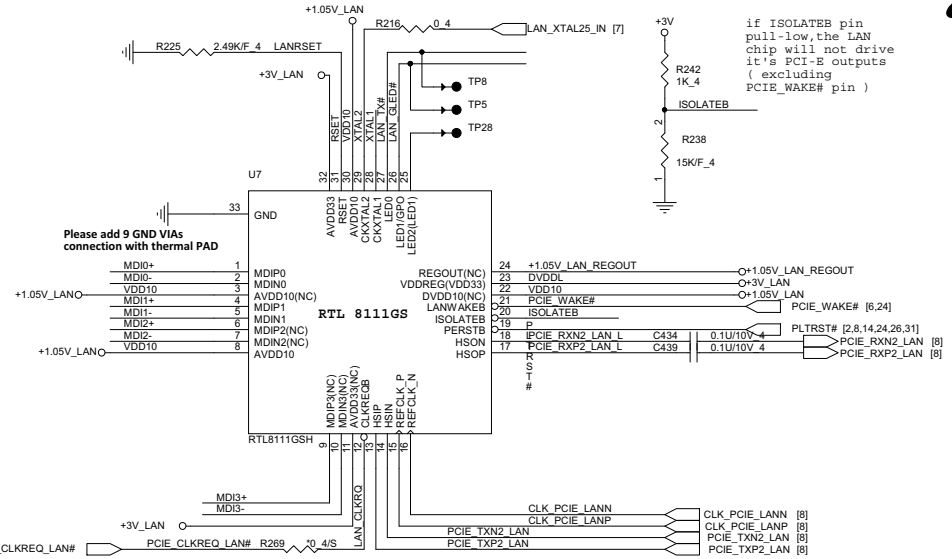
For 10/100

BOT: GST5009B LF, DB0206LAN00

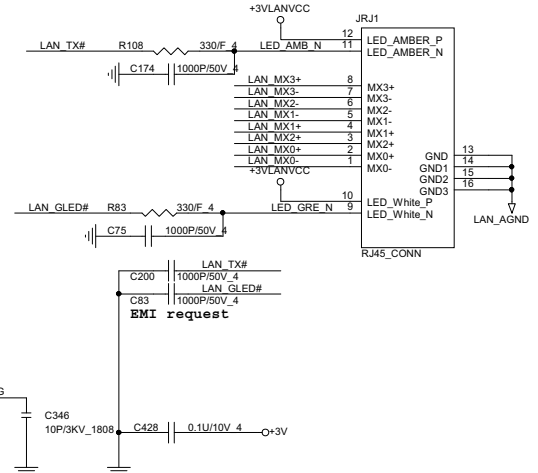
BOT: TST1284R LF DB0EL5LAN00

[2,6,7,8,9,10,12,13,14,17,18,21,22,23,24,25,26,29,30,31,36,37,39]

+3V +3VLANVCC



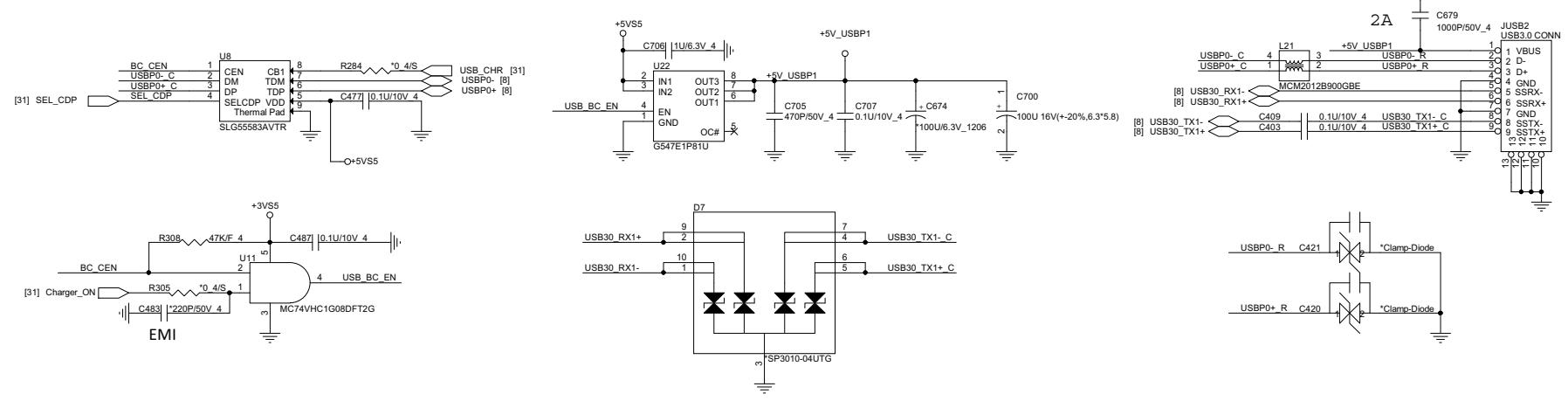
LAN conn



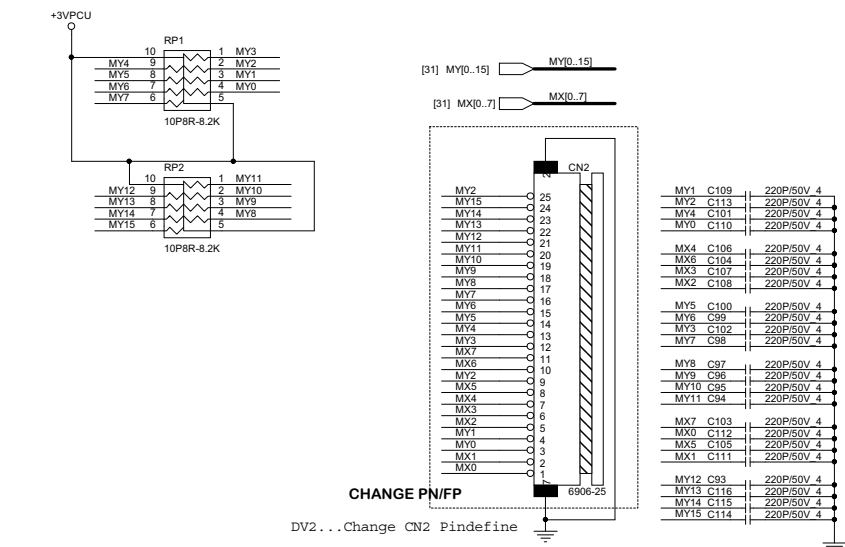
PROJECT : TWJ
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL 8111GS/RJ45	1A
Date: Friday, March 01, 2013	Sheet 27 of 42	

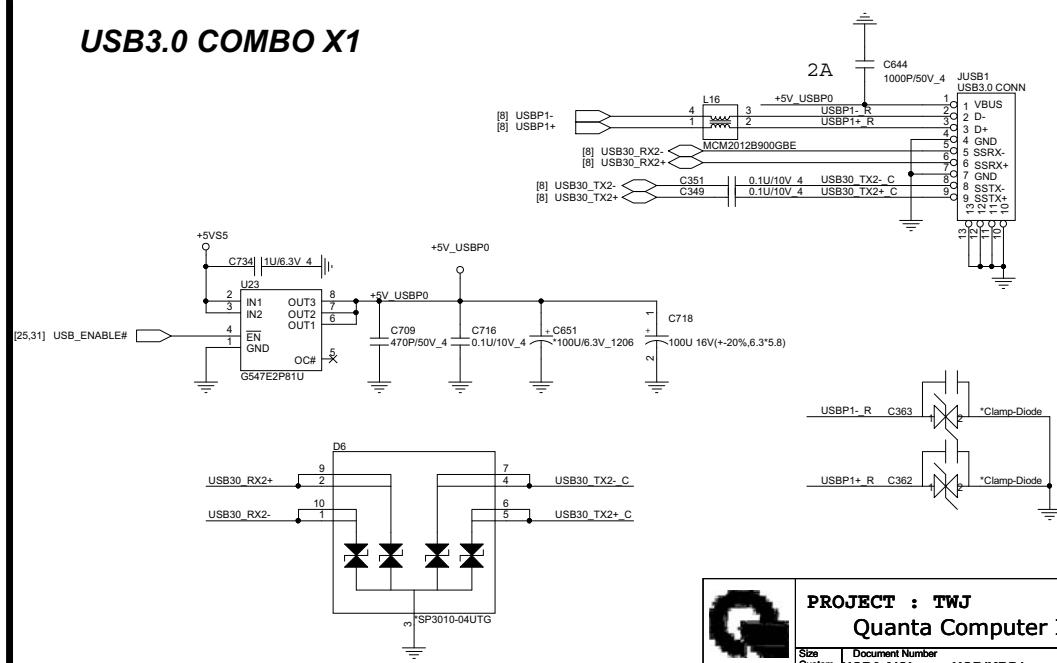
Charge USB/USB3.0 COMBO X1




Keyboard Connector



USB3.0 COMBO X1



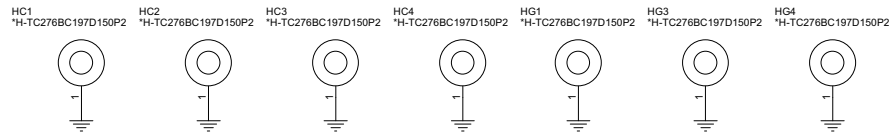


PROJECT : TWJ

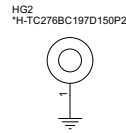
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB3.0/Charge USB/KBD/	1A
Date: Friday, March 01, 2013	Sheet 28 of 42	

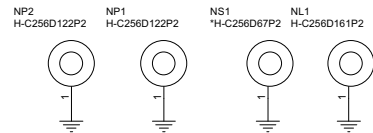
CPU Bracket



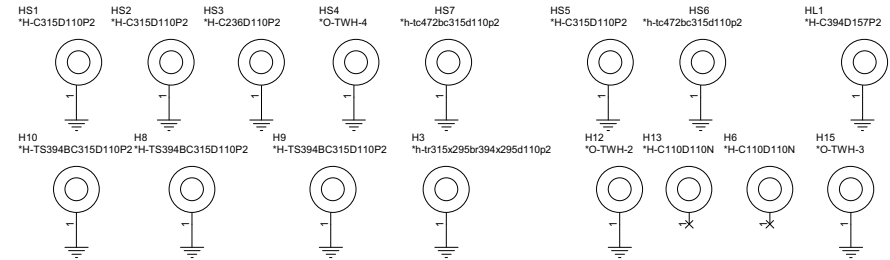
GPU Bracket



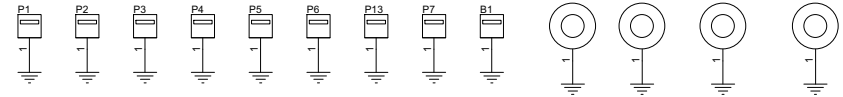
PCH NU Screw Hold



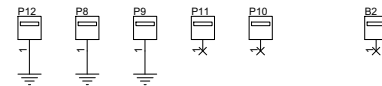
System Screw Hold



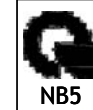
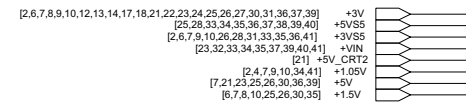
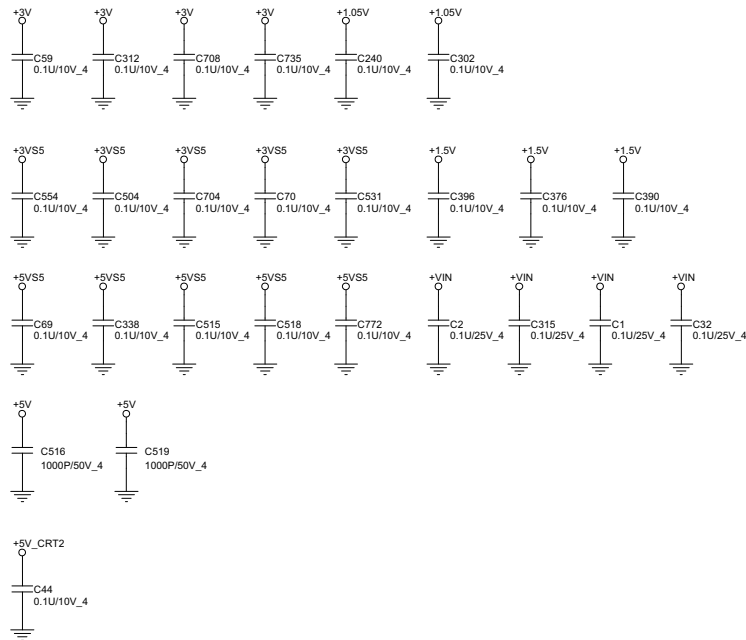
System Pad(Top)



System Pad(Button)



EMI CAP

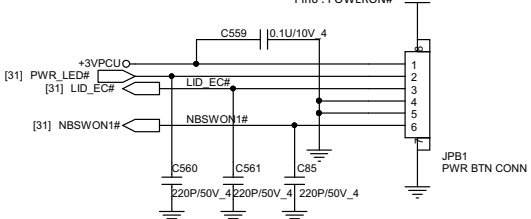


PROJECT : TWJ
Quanta Computer Inc.

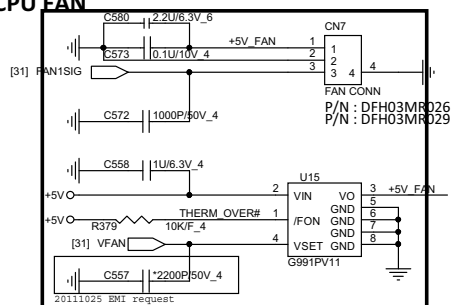
Size	Document Number	Rev
Custom	Hole / EMI Cap	1A
Date: Friday, March 01, 2013	Sheet 29 of 42	

Power Botton Connector

Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#

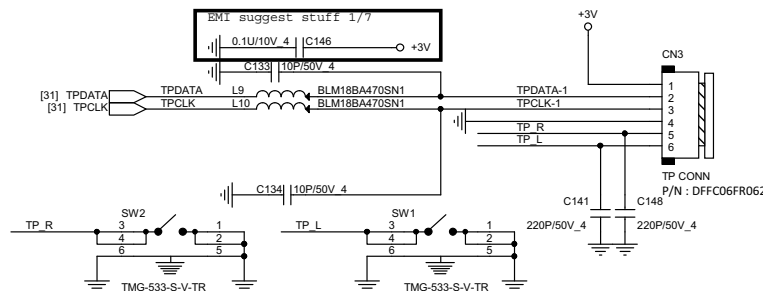


CPU FAN

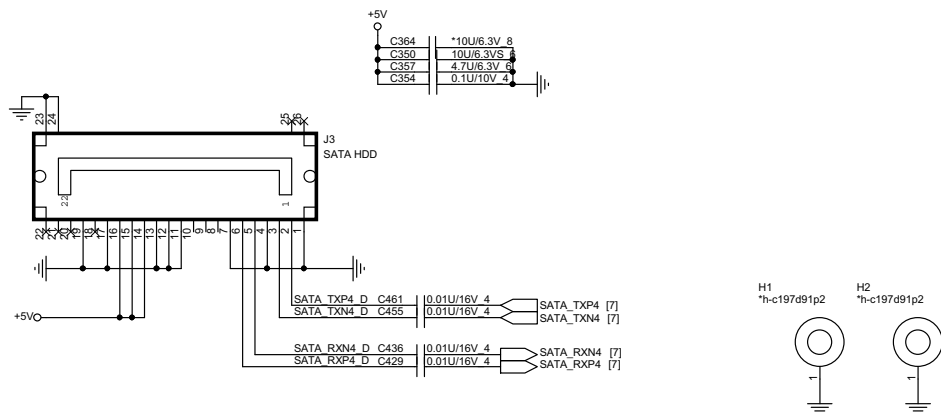


Touch Pad Connector

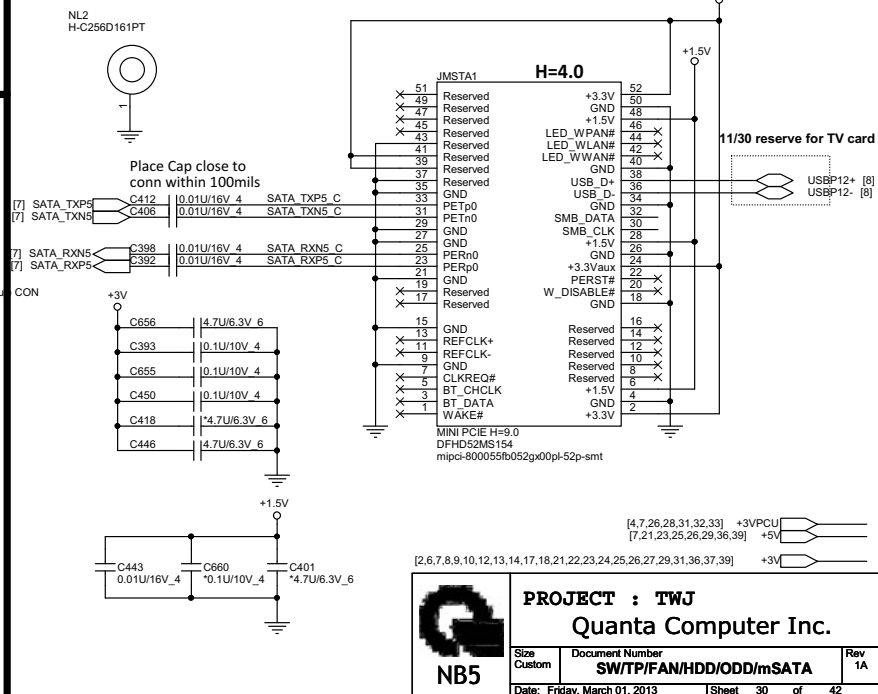
B-stage change footprint to 88513-0601-6p-l-smt



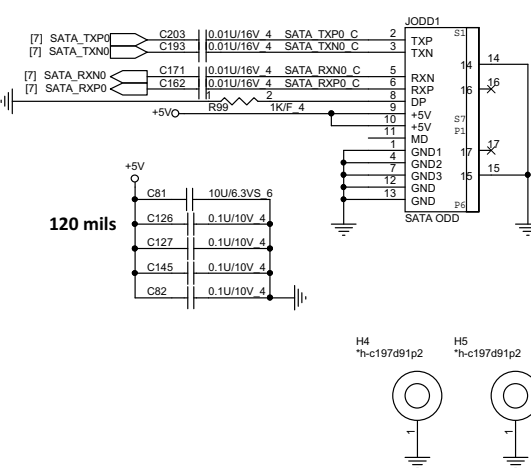
SATA HDD CONNECTOR



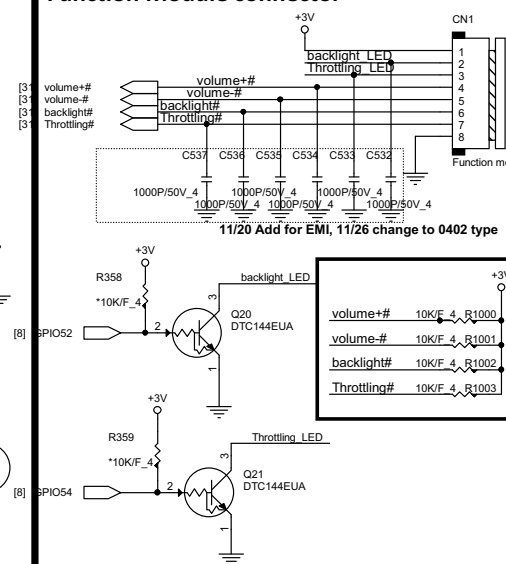
MINISATA



SATA ODD Connector

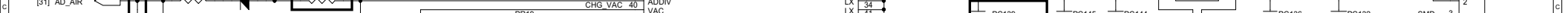


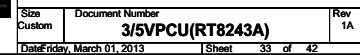
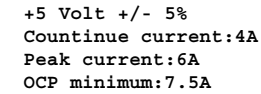
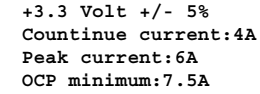
Function Module connector

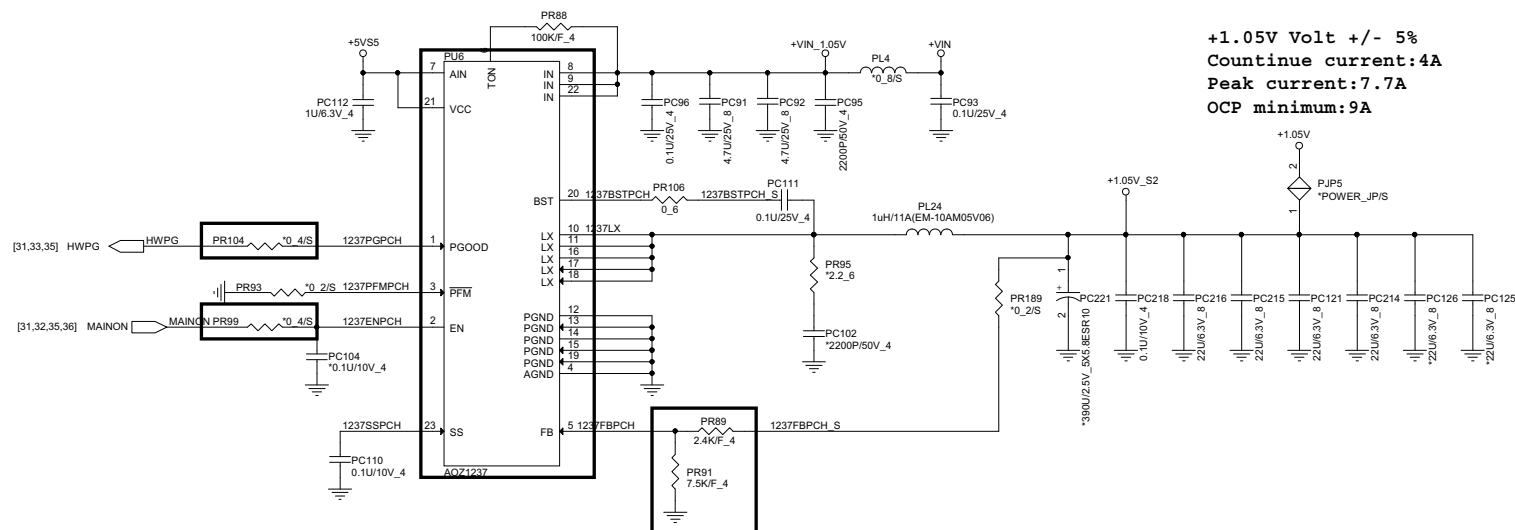


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Quanta Computer Inc.

Size Custom Document Number **SW/TP/FAN/HDD/ODD/mSATA** Rev 1A
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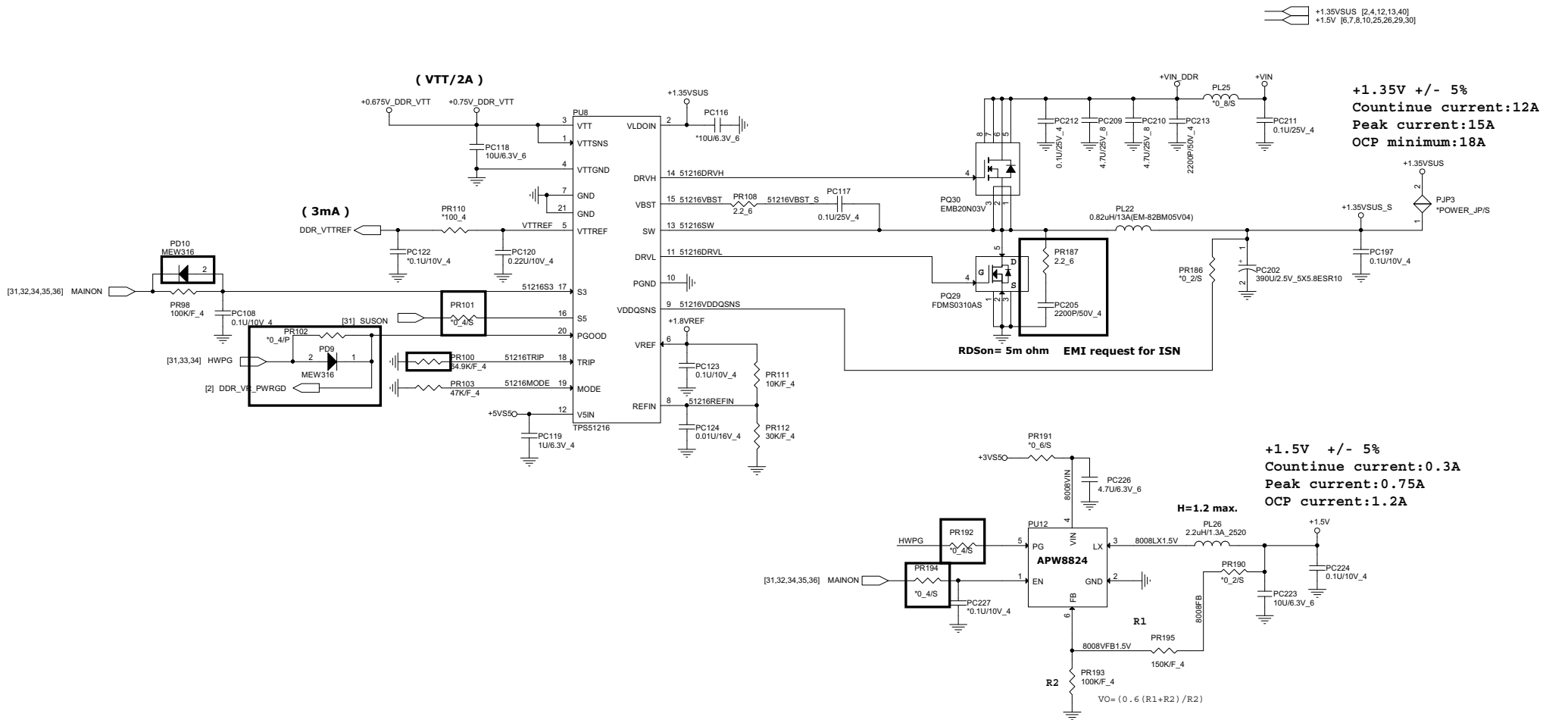


+1.05V [2,4,7,9,10,29,41]



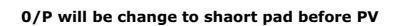
PROJECT : TWJ
Quanta Computer Inc.

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Date: Friday, March 01, 2013	Sheet 34	of 42



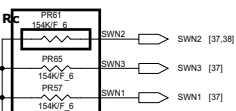
PROJECT : TWJ
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3L(APW8819)	1A
Date: Friday, March 01, 2013	Sheet	35 of 42

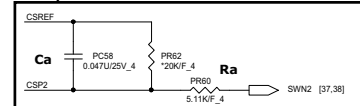


Size Custom	Document Number Dis-charge IC (G5934)	Rev 1A
Date	Friday, March 01, 2013	Sheet 36 of 42

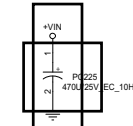
Dummy Rc For 2 phase



Dummy Ra and Ca For 2 phase



For Acoustic

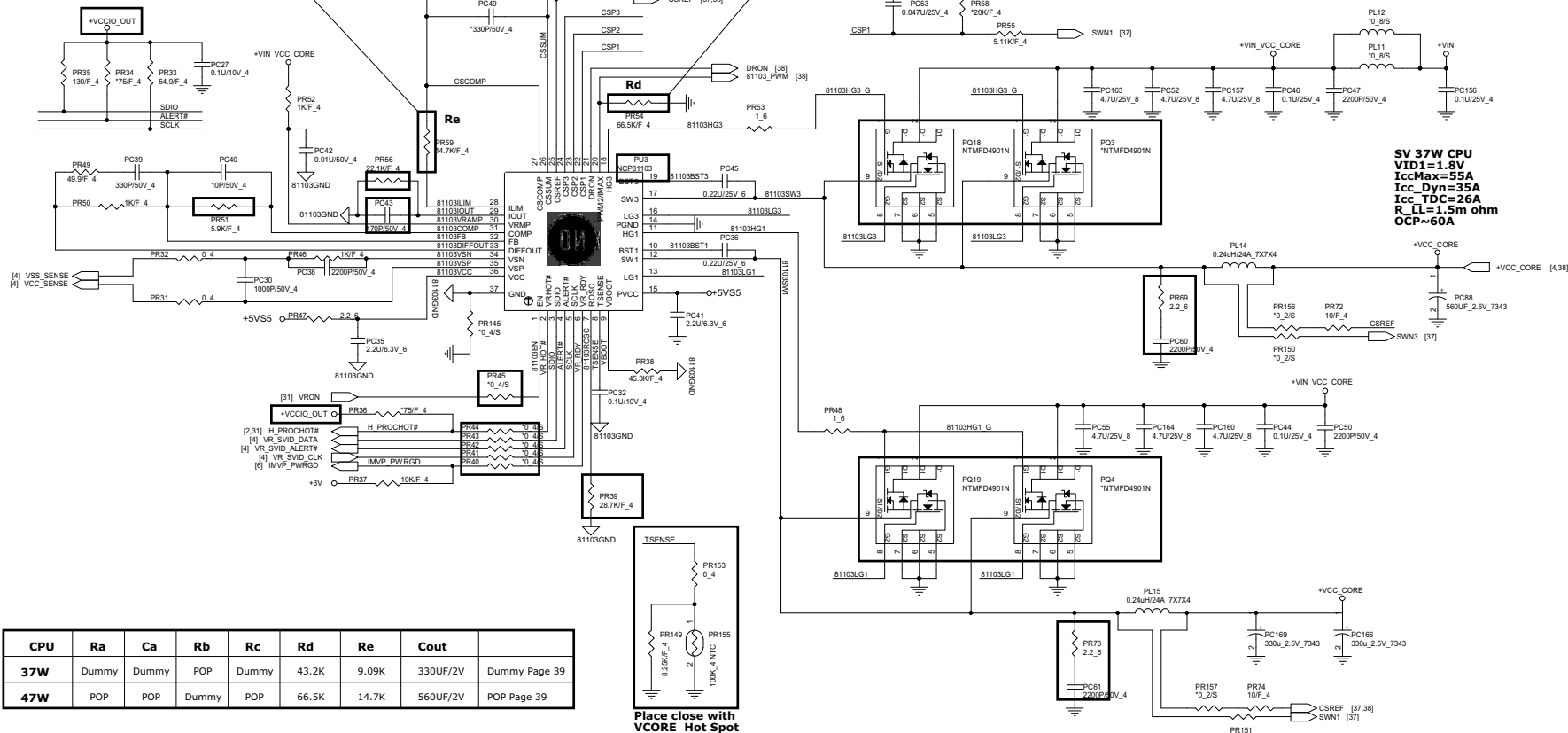
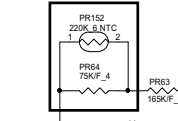


+VSS
CSP2
POP Rb for 2 phase

CPU	Re	P/N
37W	9.09K	CS29092FB27
47W	14.7K	CS31472FB14

CPU	Rd	P/N
37W	43.2K	CS34322FB00
47W	66.5K	CS36652FB16

Place close with VCORE Phase 1 Inductor



SV 37W CPU
VID1=1.8V
IccMax=55A
Icc_Dyn=35A
Icc_TDC=26A
R_LL=1.5m ohm
OCP~60A

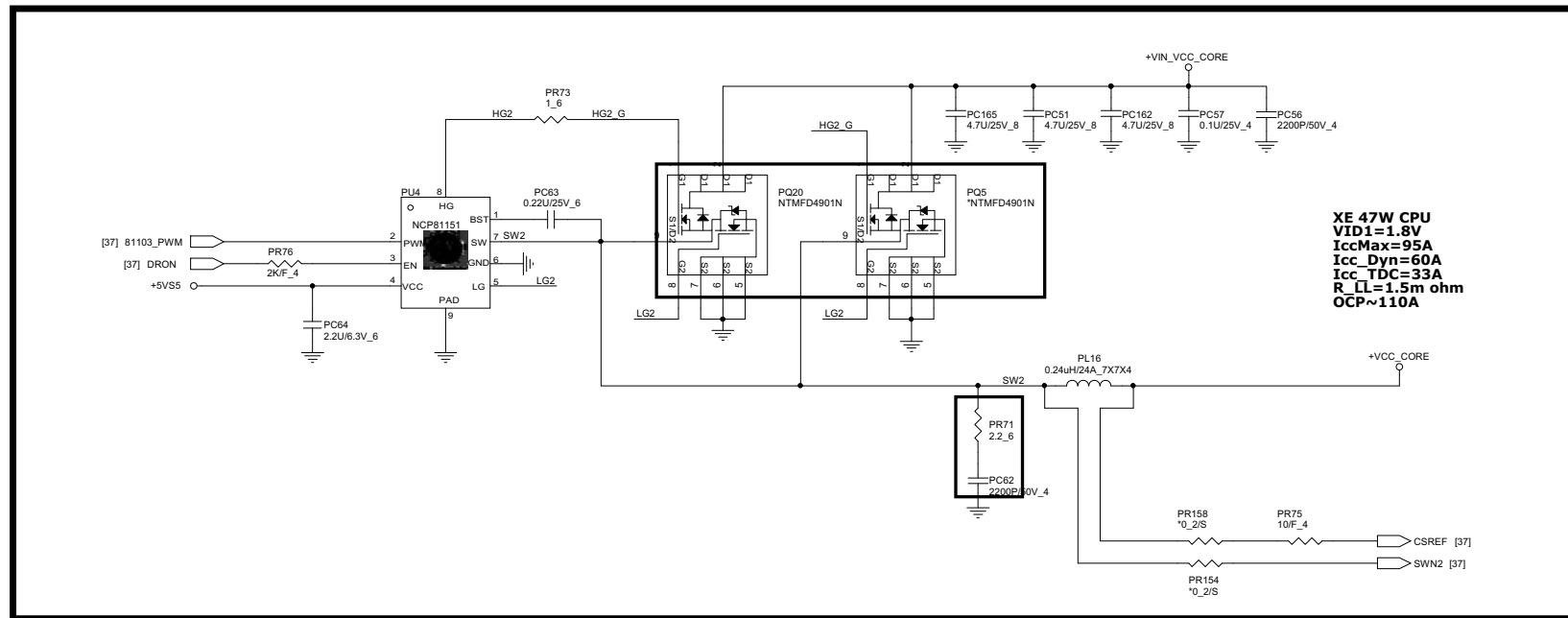
CPU	Ra	Ca	Rb	Rc	Rd	Re	Cout
37W	Dummy	Dummy	POP	Dummy	43.2K	9.09K	330UF/2V
47W	POP	POP	Dummy	POP	66.5K	14.7K	560UF/2V

Place close with VCORE Hot Spot



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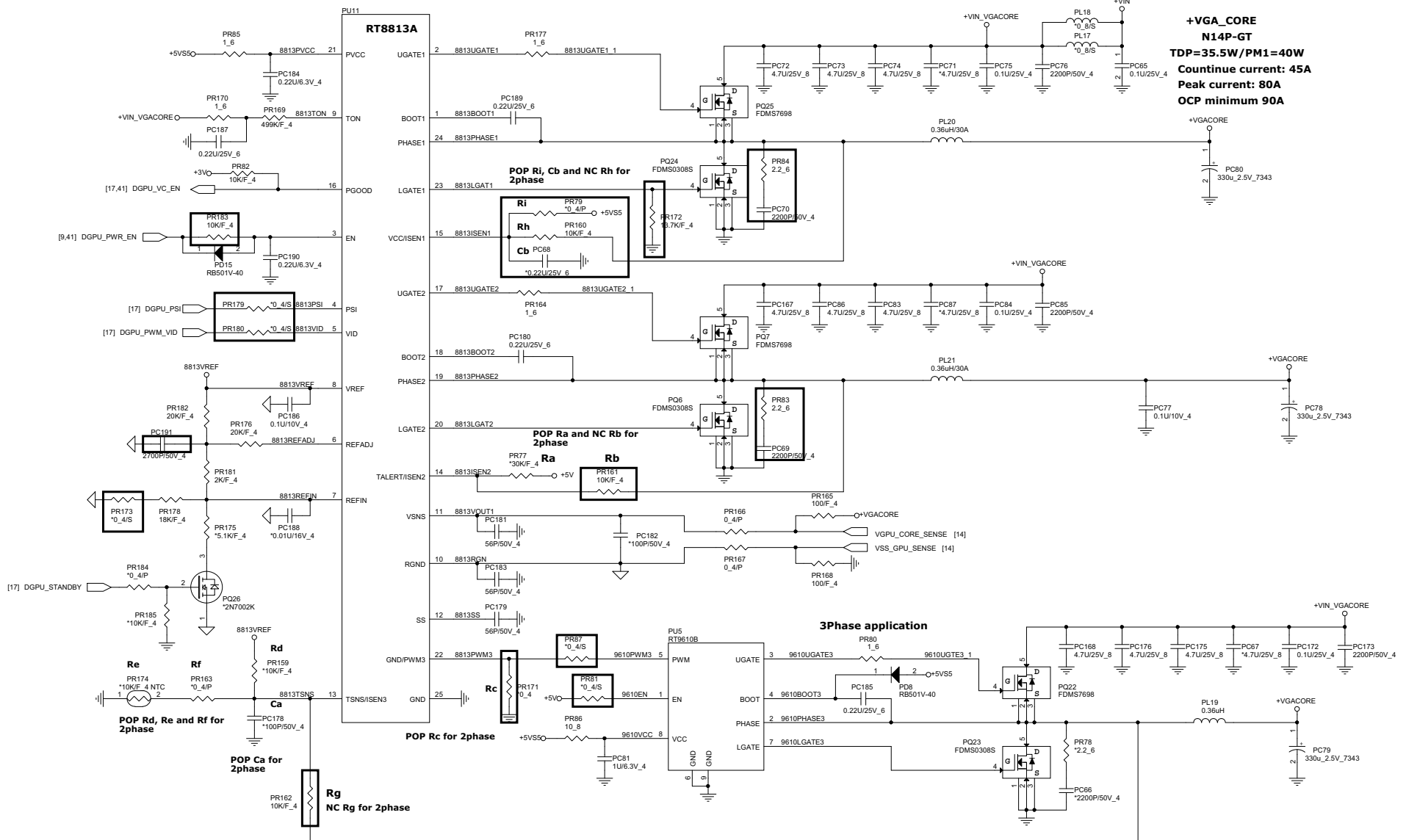


+VCC_CORE [4,37]



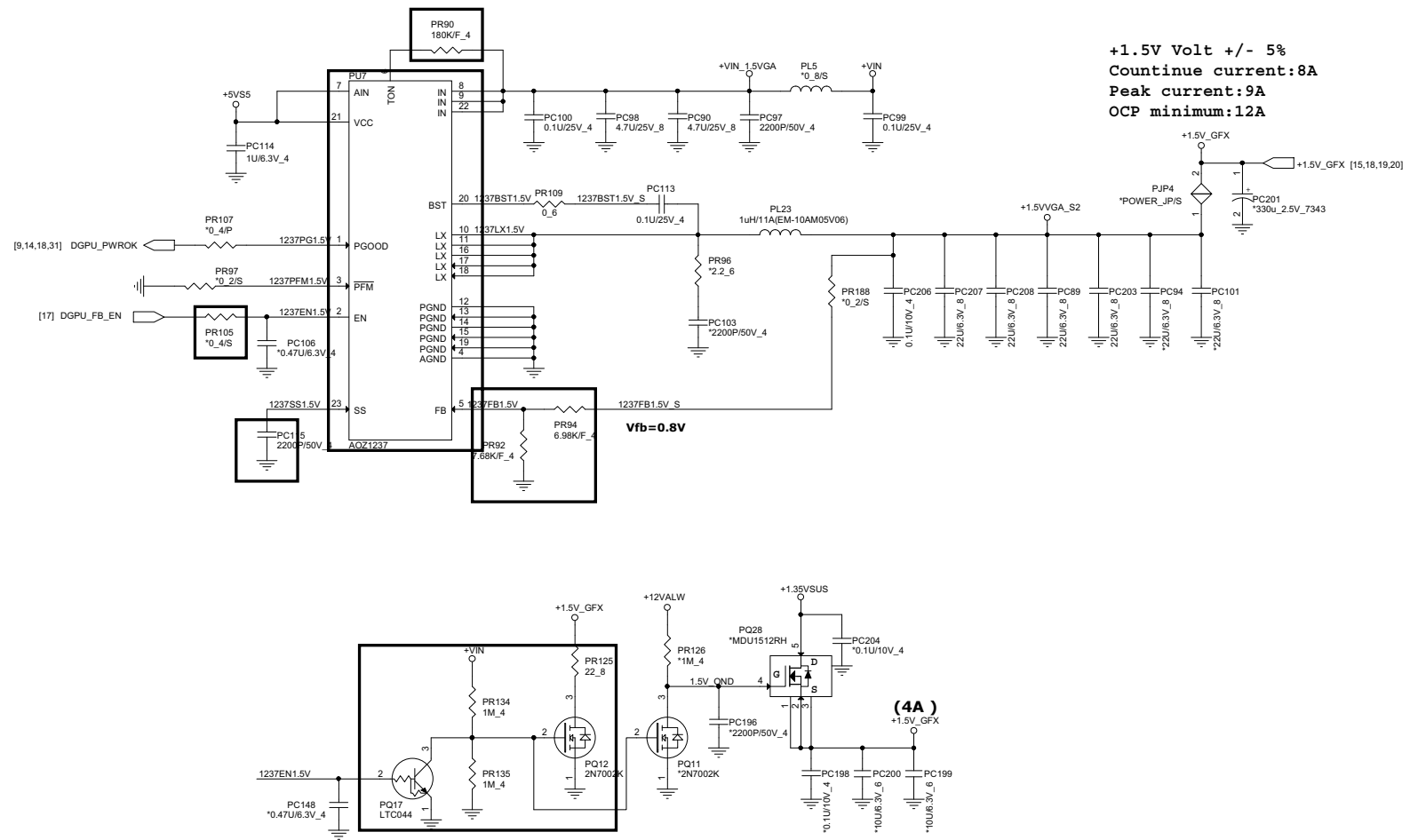
PROJECT : TWJ
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Size Custom	Document Number NCP81151	Rev 1A
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PROJECT : TWJ
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Size Custom Document Number
+VGA CORE (NCP3218G) Rev A
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PROJECT : TWJ
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Size	Document Number	Rev
Custom	+VGA POWER	A
Date: Friday, March 01, 2013	Sheet 40 of 42	

